JW5065

24V/3A

Sync. Step-Down Converter

DESCRIPTION

The JW®5065 is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 4V~24V, JW5065 delivers 3A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency.

JW5065 guarantees robustness with output short protection, thermal protection, current run-away protection and input under voltage lockout.

JW5065 is available in TSOT23-8 package, which provide a compact solution with minimal external components.

FEATURES

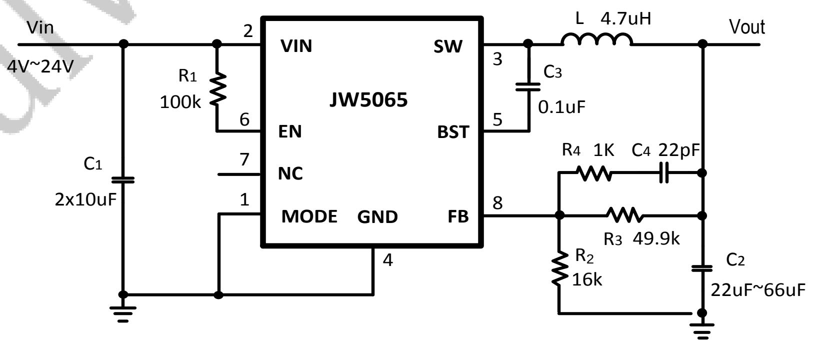
- 4V to 24V operating input range
  3A output current
- Up to 95% efficiency
- High efficiency at light load
- 450kHz switching frequency
- Internal soft-start
- Input under voltage lockout
- Current run-away protection
- Output short protection
- Thermal protection
- Available in TSOT23-8 packages

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION

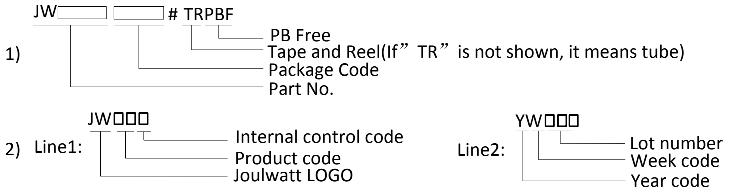
3.3V/3A Step-down Regulator



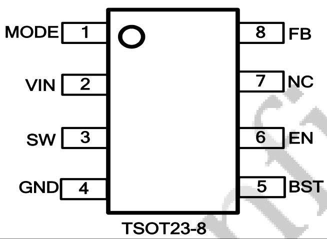
ORDER INFORMATION

DEVICE[1]	PACKAGE	TOP MARKING[2]
JW5065TSOTC#TRPBF	TSOT23-8	JW6G□ YW□□□

Notes:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, SW, MODE Pin .... -0.3V to 25V

SW Pin .... -0.3V(-6V for 10ns) to 25V (27V for 10ns)

BST Pin .... SW-0.3V to SW+5V

All other Pins .... -0.3V to 6V

Junction Temp. [2) 3)] 150ºC

Lead Temperature 260ºC

ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN .... 4V to 24V

Output Voltage Vout .... 0.8V to VIN*Dmax

THERMAL PERFORMANCE[4)]

θ_{JA} θ_{Jc}

TSOT23-8..110....55ºC/W

Note:

1) Exceeding these ratings may damage the device.

2) The JW5065 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW5065 includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN=12V, T_A=25℃, Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	3.3	3.6	3.8	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			200		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V, V_{IN} =12V			6	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1.2V		260	360	μA
Feedback Voltage	V_{FB}	4V≤V_{IN}≤24V	784	800	816	mV
Top Switch Resistance[5)]	$R_{DS(ON)T}$			70		mΩ
Bottom Switch Resistance[5)]	$R_{DS(ON)B}$			38		mΩ
Switch Frequency[5)]	F_{SW}			450		kHz
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=24V, V_{EN}=0V, V_{SW}=0V			1	μA
Bottom Switch Leakage Current[5)]	I_{LEAK_BOT}	V_{IN}=24V, V_{EN}=0V, V_{SW}=24V			1	μA
Bottom Switch Current Limit	I_{LIM_BOT}			3.3		A
Minimum On Time[5)]	T_{ON_MIN}			120		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0.4V		100		ns
EN Rising Threshold	V_{EN_H}	V_{EN} rising	1.9	2.05	2.2	V
EN Hysteresis	V_{EN_HYS}	V_{EN} Hysteresis		150		mV
Soft-Start Time[5)]	t_{SS}			1.6		ms
Thermal Shutdown[5)]	T_{TSD}			160		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYST}			20		°C

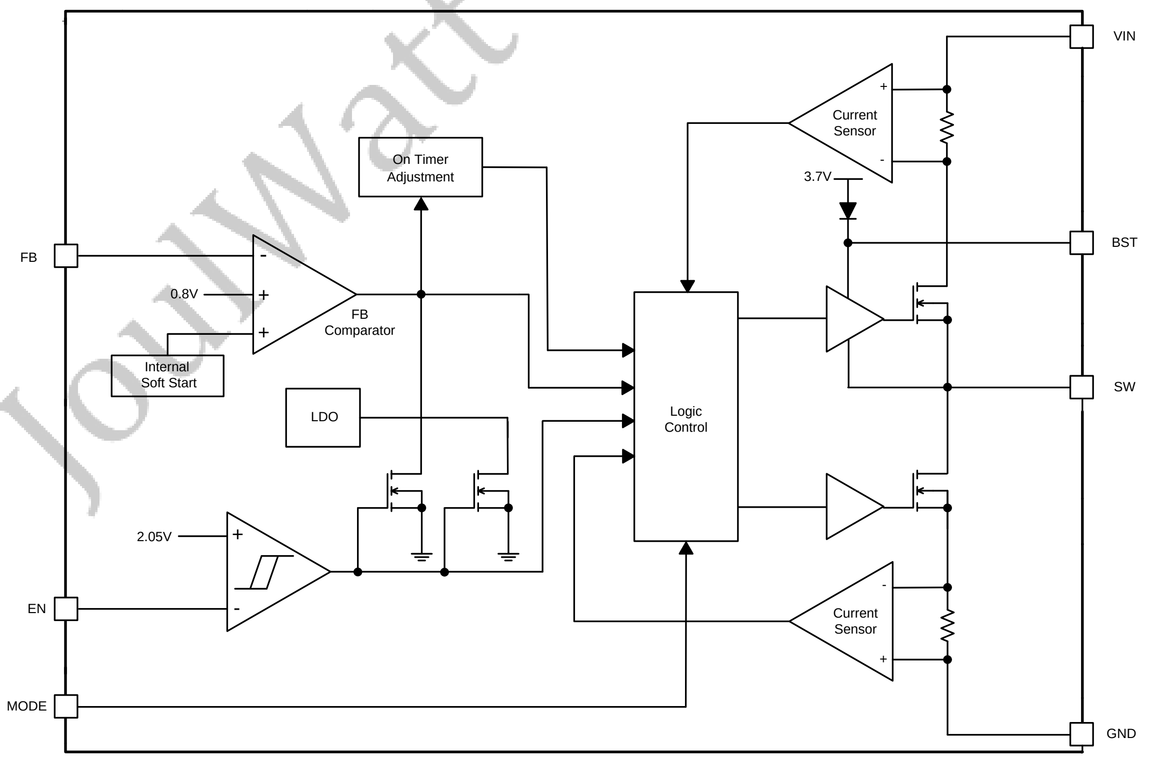
Note:

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	MODE	Pull MODE pin low to GND to achieve PFM operation. Connect MODE to VIN with 100K resistor or floating to achieve FCC operation.
2	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4V to 24V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
4	GND	Ground pin.
5	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
6	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator. Do not leave this pin floating.
7	NC	
8	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.8V. Connect a resistive divider at FB.

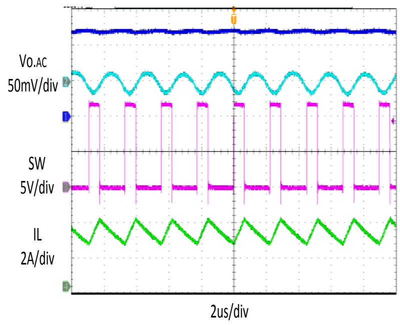
BLOCK DIAGRAM



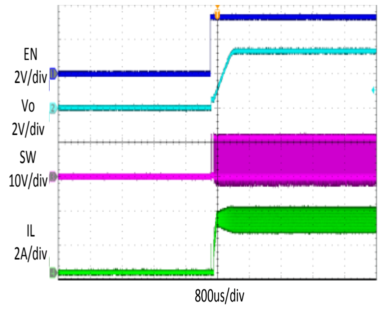
TYPICAL PERFORMANCE CHARACTERISTICS (PFM Mode)

Vin =12V, Vout = 3.3V, L = 4.7 μH, Cout = 22μF, C4=22pF,R4=1kΩ，TA = +25°C, unless otherwise noted

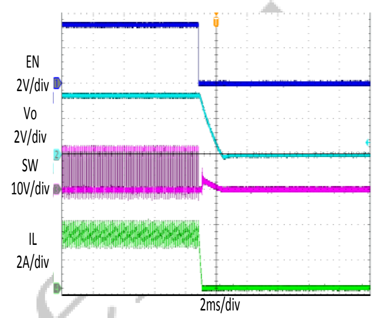
Steady State Test
VIN=12V, Vout=3.3V
Iout=3A



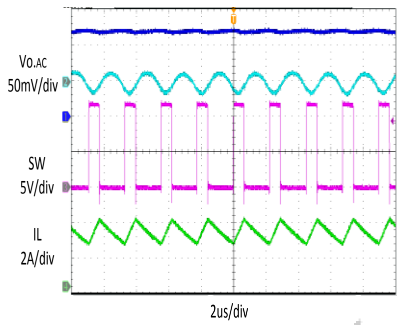
Startup through Enable
VIN=12V, Vout=3.3V
Iout=3A(Resistive load)



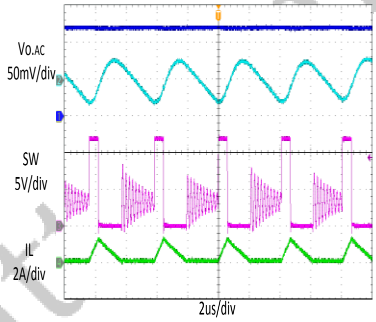
Shutdown through Enable
VIN=12V, Vout=3.3V
Iout=3A (Resistive load)



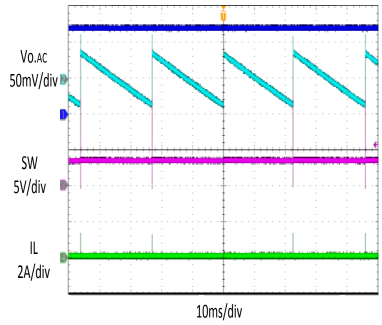
Heavy Load Operation
3A LOAD



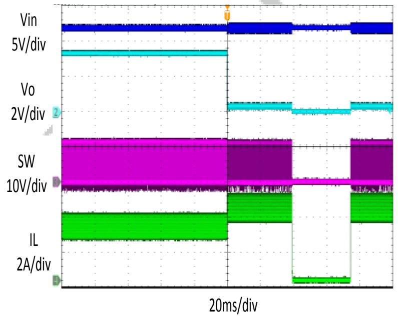
Medium Load Operation
0.3A LOAD



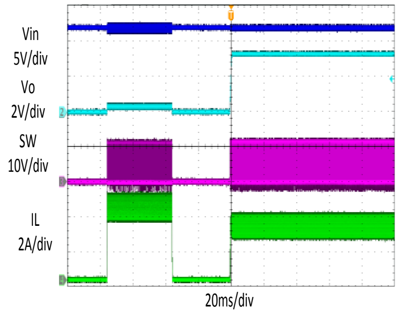
Light Load Operation
0 A LOAD



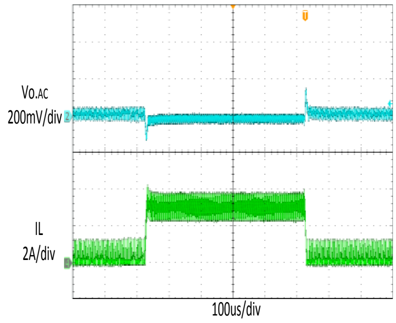
Short Circuit Protection
VIN=12V, Vout=3.3V
Iout=3A- Short



Short Circuit Recovery
VIN=12V, Vout=3.3V
Iout= Short-3A



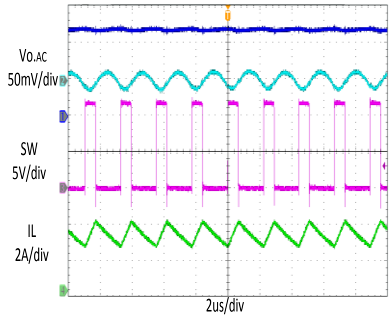
Load Transient
C4=22pF,R4=1k
0.3A LOAD → 3A LOAD → 0.3A LOAD



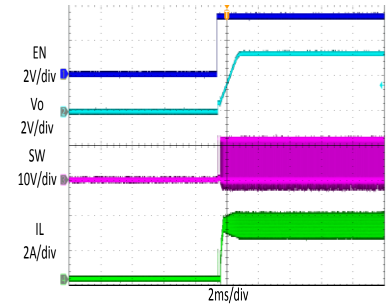
TYPICAL PERFORMANCE CHARACTERISTICS (FCC Mode)

Vin =12V, Vout = 3.3V, L = 4.7μH, Cout = 22μF, C4=22pF, R4=1kΩ，TA = +25°C, unless otherwise noted

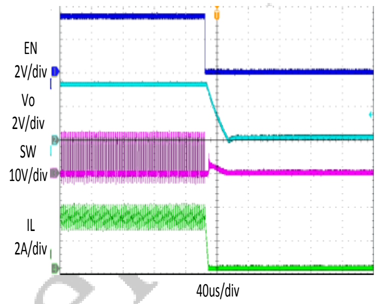
Steady State Test
VIN=12V, Vout=3.3V
Iout=3A



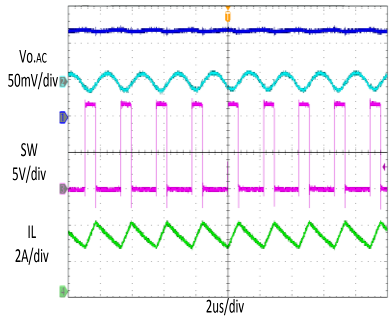
Startup through Enable
VIN=12V, Vout=3.3V
Iout=3A(Resistive load)



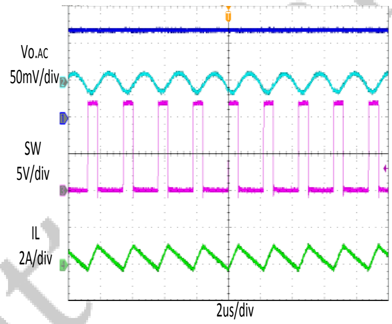
Shutdown through Enable
VIN=12V, Vout=3.3V
Iout=3A (Resistive load)



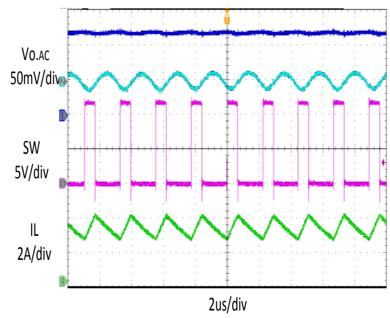
Heavy Load Operation
3A LOAD



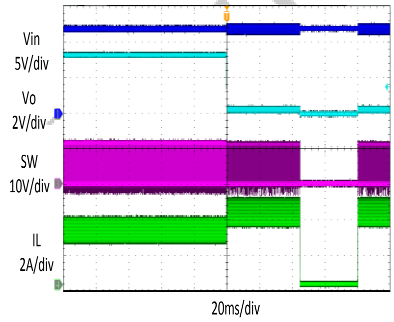
Medium Load Operation
0.3A LOAD



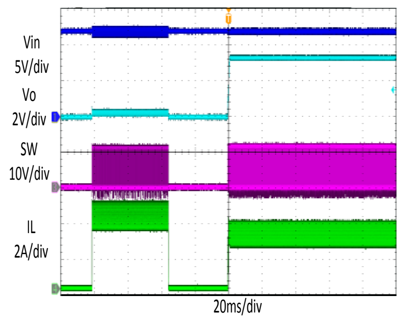
Light Load Operation
0 A LOAD



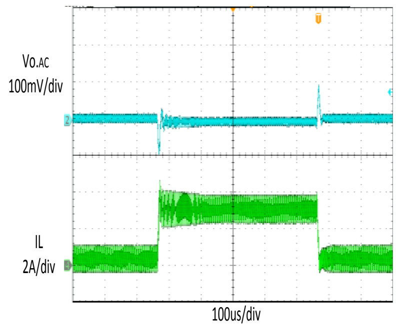
Short Circuit Protection
VIN=12V, Vout=3.3V
Iout=3A- Short



Short Circuit Recovery
VIN=12V, Vout=3.3V
Iout= Short-3A



Load Transient
C4=22pF,R4=1k
0.3A LOAD → 3A LOAD → 0.3A LOAD



FUNCTIONAL DESCRIPTION

JW5065 is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4V to 24V down to an output voltage as low as 0.8V, and is capable of supplying up to 3A of load current.

Shut-Down Mode

JW5065 shuts down when voltage at EN pin is driven below 0.3V. The entire regulator is off and the supply current consumed by JW5065 drops below 1uA.

Power Switch

N-Channel MOSFET switches are integrated on the JW5065 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.7V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and ground, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 1.9V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current.
A valley current limit is designed in JW5065 so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 1024 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 1024 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 2048 cycles. After the 2048 hiccup cycles, the regulator will try to start-up again. If the short condition still exists after 1024 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

Thermal Protection

When the temperature of the JW5065 rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 140°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_2}{R_2 + R_3}$$

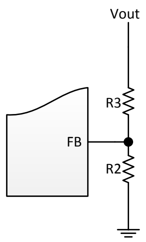
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R2 around 16kΩ, and then R3 can be calculated by:

$$R_3 = R_2 \cdot \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

VOUT(V)	R2(kΩ)	R3(kΩ)
2.5	22.1	47
3.3	16	49.9
5	20	105



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

Two pieces of 10uF/50V ceramic capacitors are recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2}\right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response, and one to three pieces of 22uF ceramic capacitor are recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

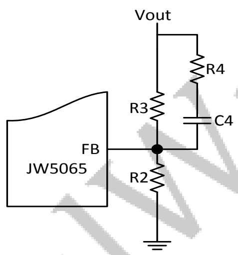
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

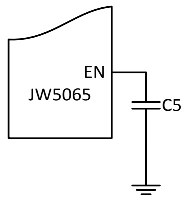
Feed-forward Capacitor

In order to minimize the ripple of output voltage at light load, a feed-forward capacitor in series with a resistor should be in parallel to the upper divider resistor. Choose R_4 around 1kΩ and C_4 around 22pF.



Start up through EN

If JW5065 start up through EN, a 10nF or larger capacitor should be connected between EN pin and GND to eliminate noise.



PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5065 (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

TSOT23-8:

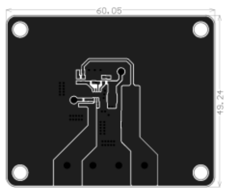


Figure 1. Top Layer

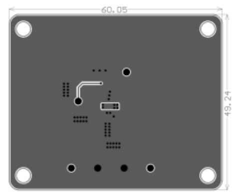


Figure 2. Bottom Layer

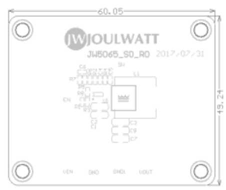
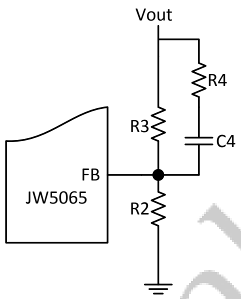


Figure 3. Top Silk Layer

External Components Suggestion:

VOUT(V)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	C4 (pF)	L(uH)	Cout(uF)
1	16	4	1	22	2.2	66
1.2	28	14	1	22	2.2	66
1.5	16	14	1	22	2.2	66
2.5	22.1	47	1	22	4.7	22~66
3.3	16	49.9	1	22	4.7	22~66
5	20	105	1	22	4.7	22~66



REFERENCE DESIGN

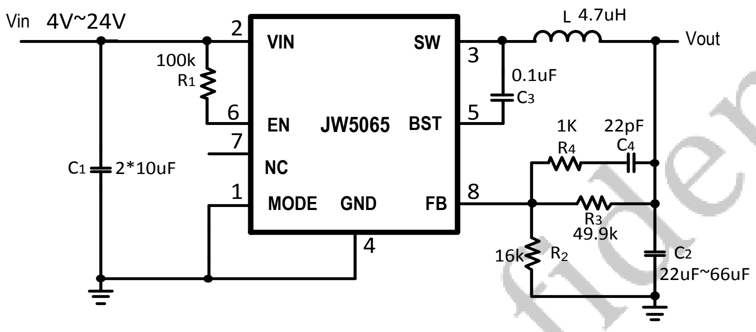
Reference 1:

Vin : 4V~24V

Vout: 3.3V

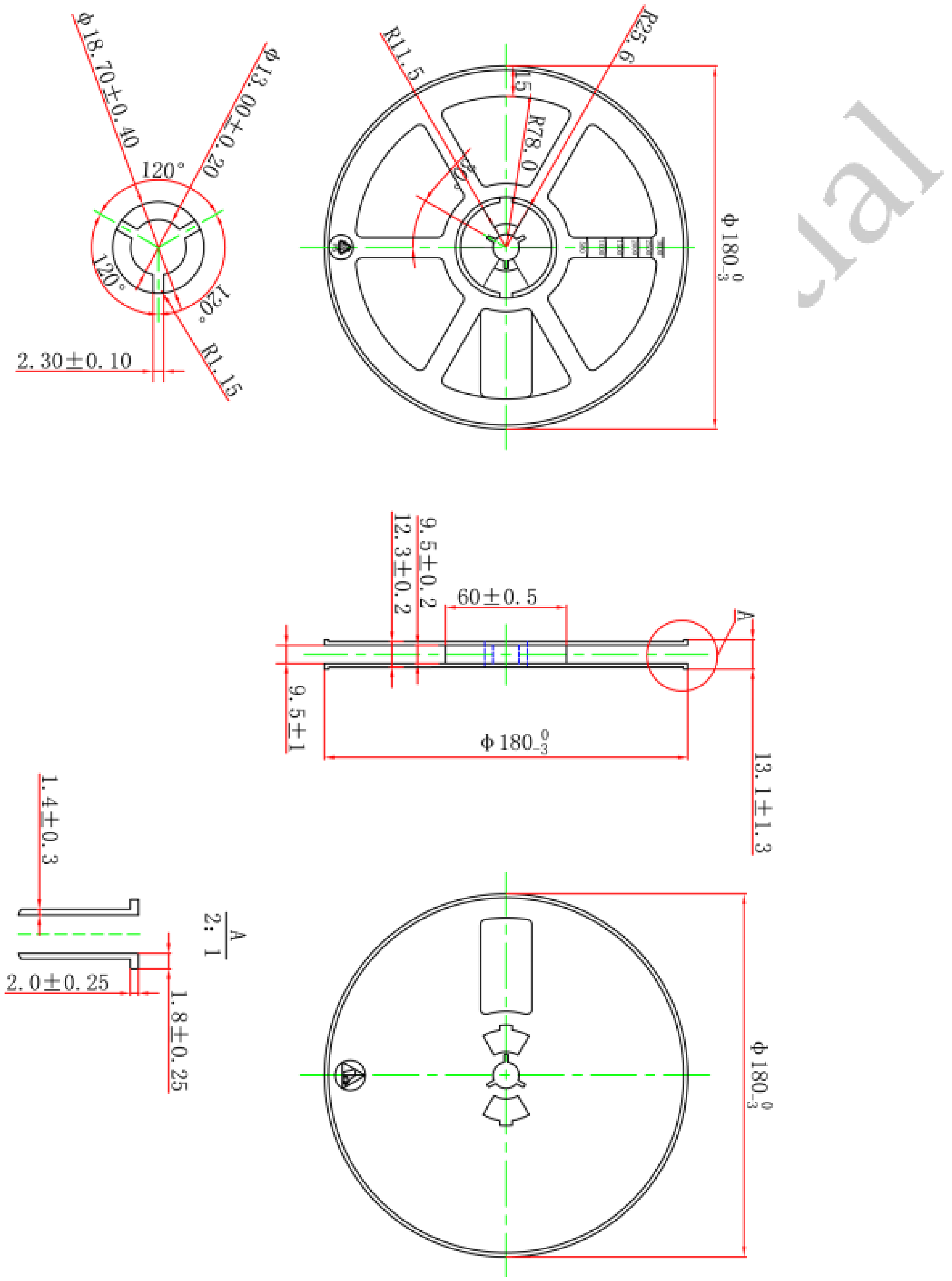
Iout : 0~3A

TSOT23-8:

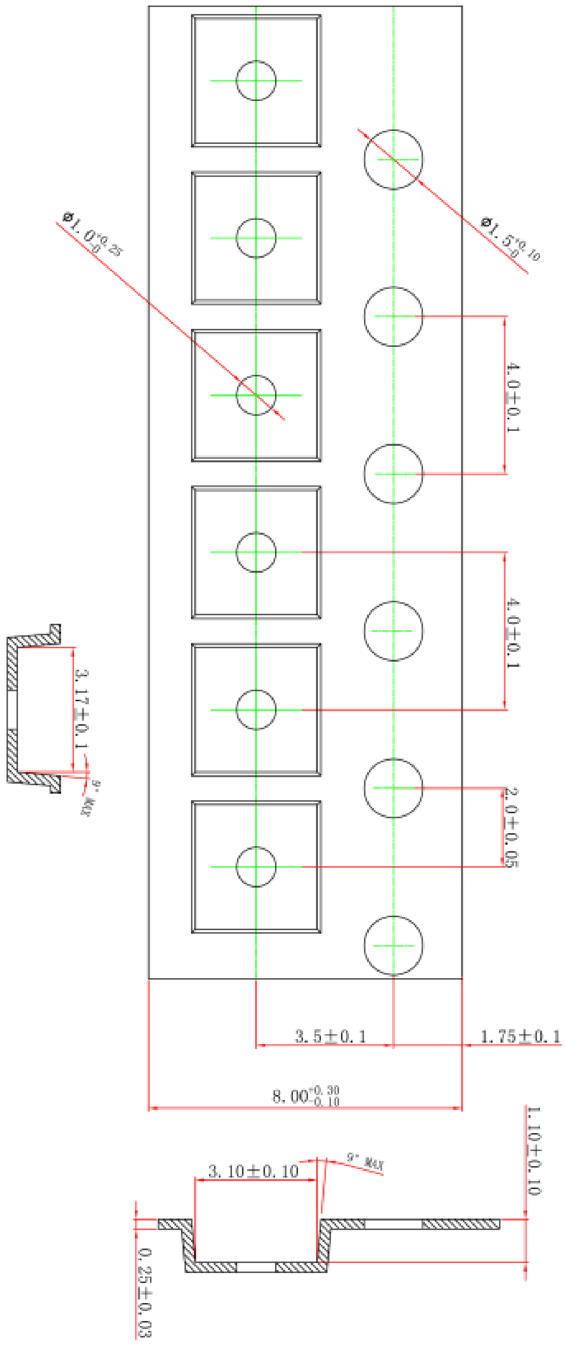


TAPE AND REEL INFORMATION

Reel UNIT: mm



Carrier Tape UNIT: mm

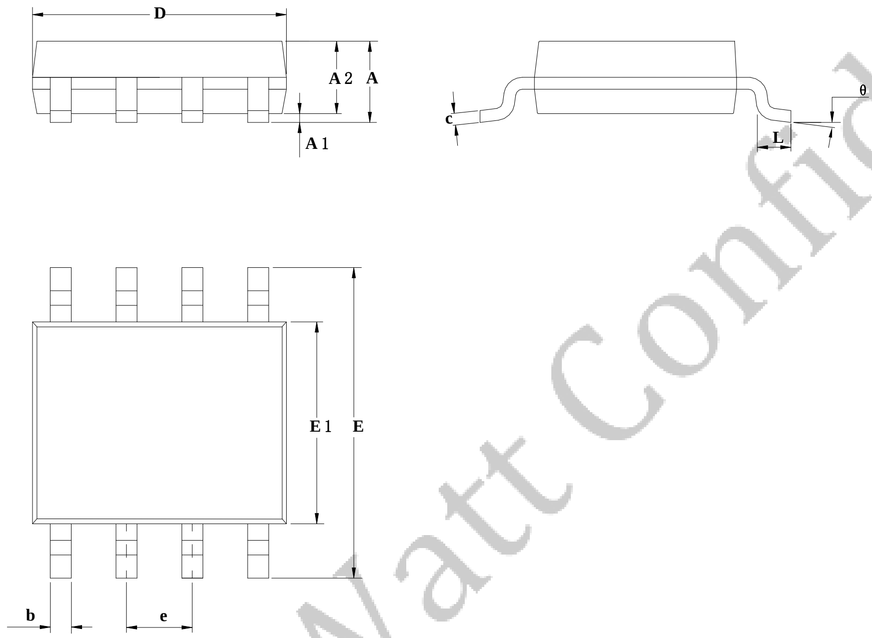


Notes:

1) COVER TAPE WIDTH: 5.50+0.20.
2) COVER TAPE COLOR: TRANSPARENT.
3) 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
4) CAMBER NOT TO EXCEED 1MM IN 100 MM.

PACKAGE OUTLINE

TSOT23-8 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.55	0.65	1.00
b	0.20	0.40	0.50
c	0.08	0.15	0.30
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.65（BSC)		
L	0.30	0.45	0.60
θ	0°	—	10°

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