JW5068C

23V/8A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5068C is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 5.5V~23V, JW5068C delivers 8A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripples.

JW5068C guarantees robustness with output short protection, thermal protection, current run-away protection, and input under voltage lockout.

JW5068C is available in QFN3×3-20 package, which provide a compact solution with minimal external components.

FEATURES

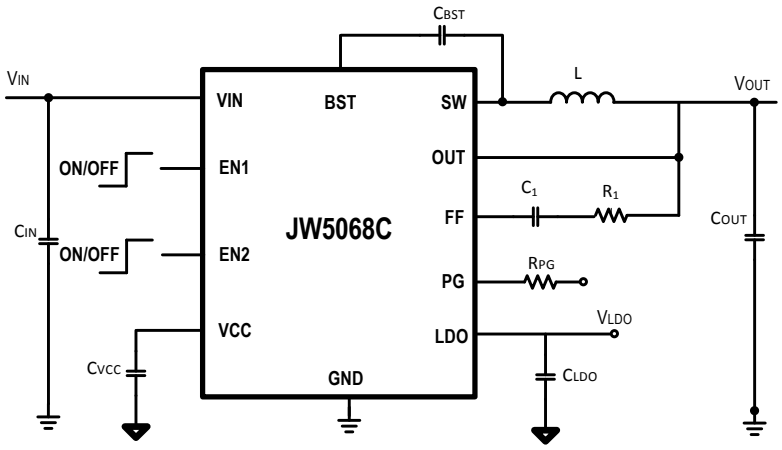
- 5.5V to 23V operating input range
  8A output current
- Up to 95% efficiency
- High efficiency at light load
- 600kHz frequency
- Input under voltage lockout
- Power good indicator
- Output discharge function
- Output Over/Under Voltage Protection
- Output short protection
- Thermal protection
- Available in QFN3X3-20 package

APPLICATIONS

- Industrial and commercial low power system
- Computer peripherals
- LDO monitors and TVs
- Green Electronics/ Appliances

TYPICAL APPLICATION

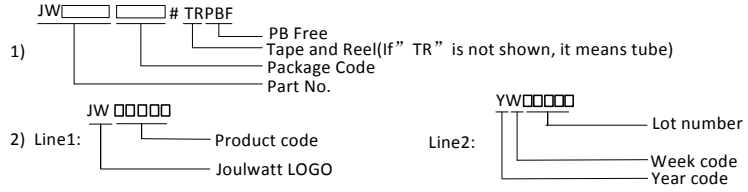
8A Step-down Regulator



ORDER INFORMATION

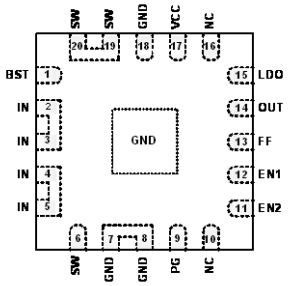
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW5068CQFNF#TRPBF	QFN3X3-20	JW5068C YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN1,EN2, PG, SW Pin..... -0.3V to 28V
BST Pin ..... SW-0.3V to SW+5V
All other Pins ..... -0.3V to 6V
Junction Temp. [2)] 150ºC
Lead Temperature 260ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN ..... 5.5V to 23V
Output Voltage Vout 5.1V
Ambient Temperature Range ..... -40°C to 85°C

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
QFN3X3-20	30	4.5ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW5068C includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN=12V, T_A=25℃, Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	4.25	4.48	4.7	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Current 1	I_{SD1}	EN1=0, EN2=1			100	μA
Shutdown Current 2	I_{SD2}	EN1=0, EN2=0		2	6	uA
Supply Current	I_Q	V_{EN}=5V, V_{OUT}=5.2V		36	48	μA
EN1 Input High Voltage	V_{EN1_H}		0.8	-	-	V
EN1 Input Low Voltage	V_{EN1_L}		-	-	0.4	V
EN2 Input High Voltage	V_{EN2_H}		0.8	-	-	V
EN2 Input Low Voltage	V_{EN2_L}		-	-	0.4	V
Output Voltage Setpoint	V_{SET}	5.5V<V_{VIN}<23V	5.023	5.1	5.177	V
Top Switch Resistance	$R_{DS(ON)T}$			20		mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			10		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=23V, V_{SW}=0V			1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=23V, V_{SW}=23V			3	μA
Top Switch Current Limit[5)]	I_{LIM_TOP}		14.8	16	17.2	A
Bottom Switch Current Limit	I_{LIM_BOT}		8	10	12	A
Minimum On Time[5)]	T_{ON_MIN}			100		ns
Minimum Off Time[5)]	T_{OFF_MIN}			100		ns
Switching Frequency [5)]	Fs			600		kHz
Discharge FET Ron	R_{DIS}			15		Ω
Soft-Start Time[5)]	T_{SS}			0.8		ms
Power Good Threshold	$PGD_{\_TH}$	V_{OUT} Rising	88.5%	92.5%	96.5%	V_{SET}
Power Good Hysteresis[5)]	$PGD_{\_HYS}$			8%		V_{SET}
Power Good Delay Time[5)]		Low to high		350		us
		High to low		10		us
Power Good Sink Current	I_{PG}	PG=0.5V	2			mA
Output Over-voltage Threshold		V_{OUT} Rising	115%	120%	125%	V_{SET}
Output Over-voltage Hysteresis[5)]				5%		V_{SET}
Output Over-voltage Delay Time[5)]				20		us
Output Under-voltage Threshold[5)]		V_{OUT} Falling	60%	65%	70%	V_{SET}
Output Under-voltage Delay Time[5)]		V_{OUT} forced below UV threshold		100		us
LDO Output Voltage[5)]	V_{LDO1}	VIN=12V, I_{LDO}=100mA@EN1=EN2=1	4.9	5	5.1	V

VIN=12V, T_A=25℃，Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
LDO Output Voltage	V_{LDO2}	VIN=12V, I_{LDO}=100mA@EN1=0,EN2=1	4.75	5	5.25	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=25mA		200		mV
LDO Output Current Limit	I_{LMTLDO}		205	260	320	mA
Bypass Switch Ron	R_{BYP}			3		Ω
Bypass Switch Turn-on Voltage	V_{BYP_ON}		4.4	4.7		V
Bypass Switch Switchover Hysteresis	V_{BYP_HYS}			0.12		V
Thermal Shutdown[5)]	T_{TSD}			150		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYST}			15		°C

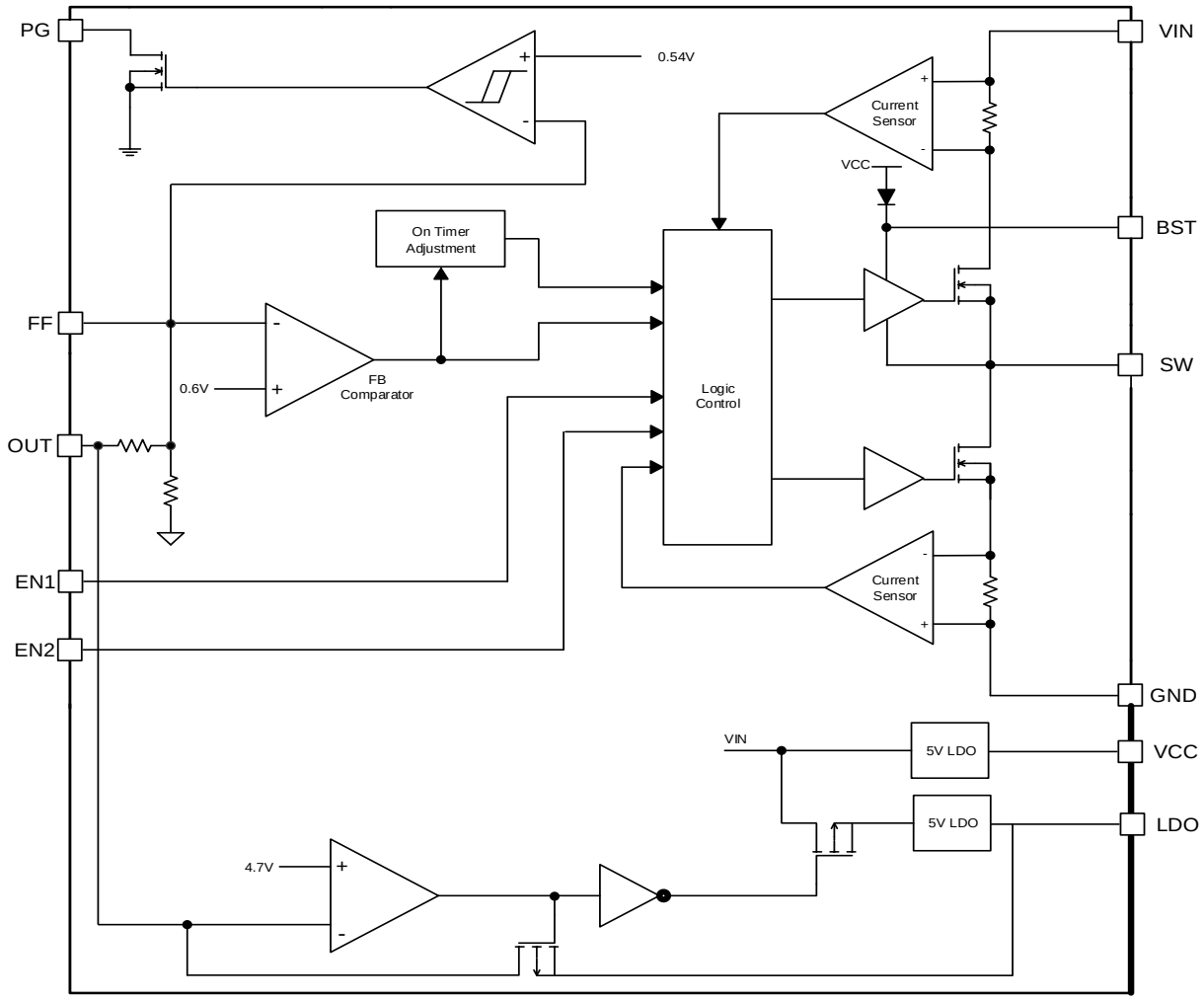
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2,3,4,5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 5.5V to 23V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6,19,20	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
7,8,18,EP	GND	Ground pin
9	PG	Power good monitor output. Open drain output when the output voltage is within 93% to 120% of regulation point.
11	EN2	Enable control of the IC and internal LDO. Pull this pin high to turn on the IC and internal LDO. Do not leave this pin floating.
10, 16	NC	
12	EN1	Enable control of the DC-DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating
13	FF	Output feed forward pin. Connect RC network from the output to this pin.
14	OUT	Output pin. Connect to the output of DC-DC regulator. The pin also provide the bypass input for 5V LDO.
15	LDO	5V LDO Output. Decouple this pin to ground with at least 4.7uF ceramic capacitor.
17	VCC	Internal 5V LDO Output. Power supply for internal analog circuits and driving circuit. Decouple this pin to ground with a 2.2uF ceramic capacitor.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW5068C is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 5.5V to 23V down to a 5.1V output voltage, and is capable of supplying up to 8A of load current.

Power Switch

N-Channel MOSFET switches are integrated on the JW5068C to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 4.7V rail when SW is low.

Vin Under-Voltage Protection

In addition to the enable function, the JW5068C provides an Under Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Soft Start

The JW5068C has an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 0.8ms.

Enable and Disable

The JW5068C's EN1 and EN2 is used to control converter, the enable voltage (EN1 and EN2) both have low and high threshold voltage. When both VEN1 and VEN1 are below its low threshold voltage, the IC enters shutdown mode. When both VEN1 and VEN2 exceed its high threshold voltage, the converter is fully operational. When VEN1 is below this level and VEN2 exceeds its high threshold voltage, the regulator is off and the LDO is on.

Power Good

The JW5068C has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to Vcc or another voltage source through a resistor. It is high if the output voltage is higher than 93% or lower than 120% of the nominal voltage.

Output Voltage Over-voltage Protection

JW5068C integrates both output over-voltage protection and under-voltage protection. If the output voltage rises above the regulation level, the high-side MOSFET naturally remains off and the synchronous rectifier will turn on until the inductor current reaches the zero. If the output voltage exceeds the OVP threshold for longer than 20 us (typical), the OVP function is triggered. If the output voltage drops below the UVP trip threshold for longer than 200 us (typical), the UVP function is triggered.
JW5068C use latch-off mode in OVP and UVP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Linear Regulators (LDO & VCC)

The JW5068C integrates a 5V linear regulator (LDO). The regulators can supply up to 200mA for external load, therefore it' s recommended to bypass LDO with a minimum 4.7uF ceramic capacitor to GND. When the voltage of OUT pin

is higher than the switch over threshold 4.7V, an automatic circuit will change the power source of linear regulator from VIN path to external path, therefore the power dissipation of linear regulator will be decrease efficiently.

The JW5068C also integrates a 5V linear regulator (VCC). The VCC regulator steps down input voltage to supply both internal circuitry and gate drivers. Do not connect the VCC pin to external loads.

Thermal Protection

When the temperature of the JW5068C rises above 150°C, it is forced into thermal protection (OTP). The JW5068C uses latch-off mode in OTP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again.

APPLICATION INFORMATION

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.
Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_S * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage. The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.
A 10uF*4 ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * \left(R_{ESR} + \frac{1}{8 * f_S * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response, and a 66uF~88uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

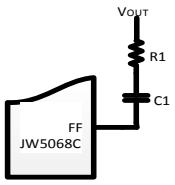
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

Feedforward Capacitor

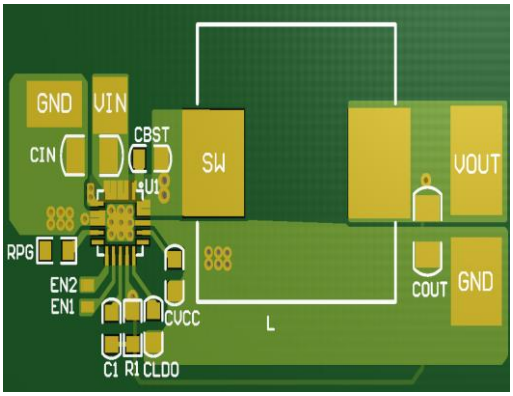
In order to minimize the ripple of output voltage at load transient, a feedforward capacitor in series with a resistor should be in parallel to the upper divider resistor. Choose R_1 around 0Ω and C1 around 50pF.



PCB Layout Note

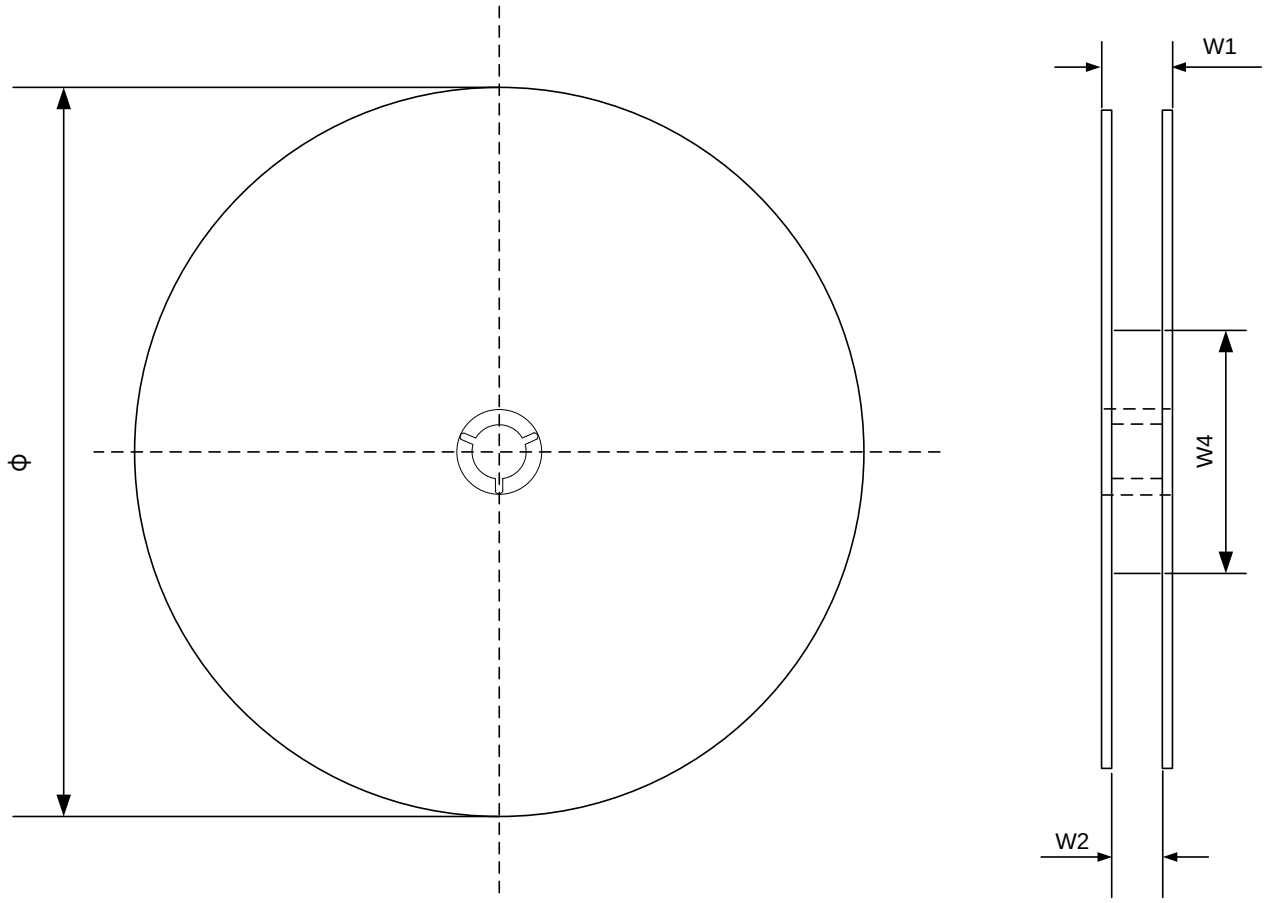
For minimum noise problem and best operating performance, We should place the following components close to the IC: C_{IN}, C_{LDO} and L.

1. Place the input decoupling capacitor as close to JW5068C (VIN pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.



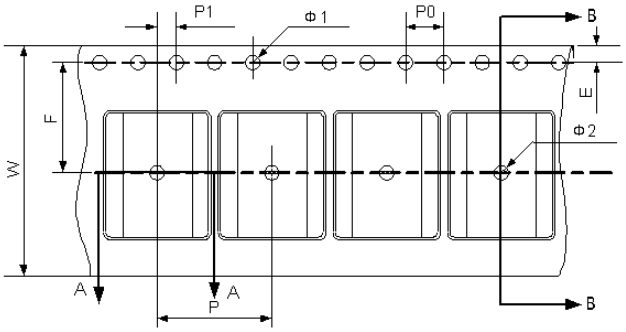
TAPE AND REEL INFORMATION

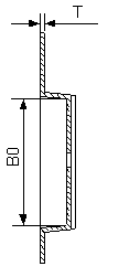
Reel UNIT: mm



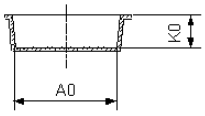
封装形式	直径 Φ	厚度 W1	宽度 W2	W4
QFN3×3-20	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm



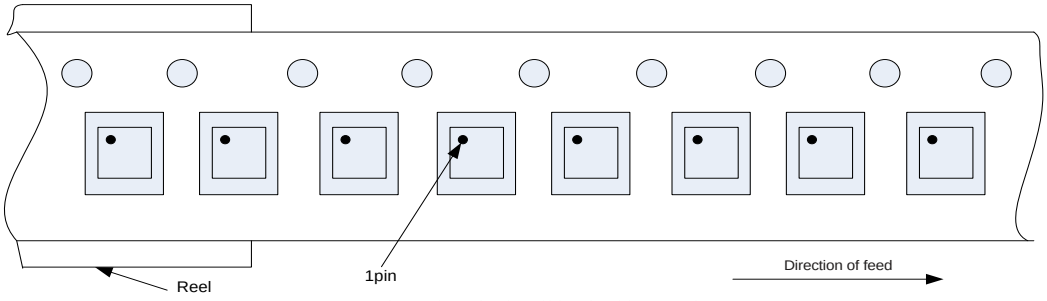


SECTION B-B



SECTION A-A

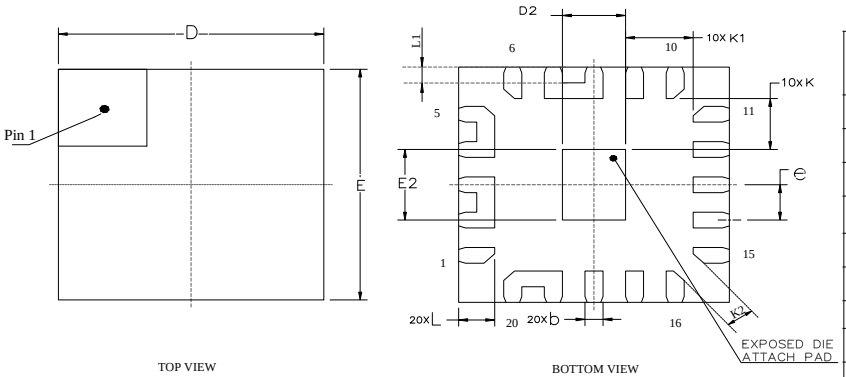
封装形式	P0	P1	P	A0	B	W	T0	K0	Φ1	Φ2	E	F
QFN3x3-20	4.0±0.1	2.0±0.1	8.0±0.2	3.30±0.2	3.30±0.2	12.0±0.3	0.25±0.20	0.75±0.2	1.50min	1.50min	1.75±0.1	5.50±0.10

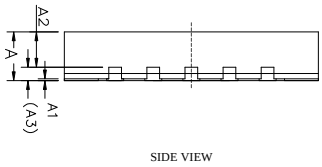


*Order quantity needs to be multiple of the minimum quantity.

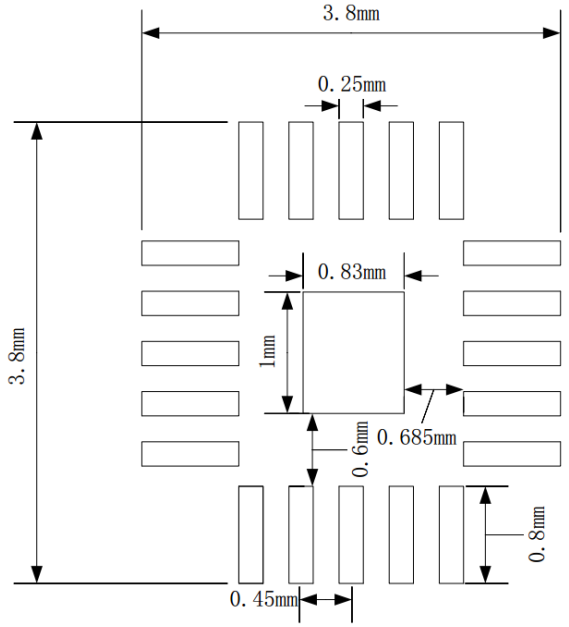
PACKAGE OUTLINE

QFN3X3-20 UNIT: mm





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
A2	---	0.40	---
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
e		0.45 BSC	
D2	0.60	0.70	0.80
E2	0.80	0.90	100
L	0.30	0.40	0.50
L1		0.20 REF	
K		0.65 REF	
K1		0.75 REF	
K2		0.311 REF	



Recommended PCB layout
(Reference only)

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