JW7211

-48V Hot Swap and Single ORing Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®7211 is an integrated hot swap and ORing controller that enables high power telecom systems to comply with stringent transient requirements. The 200-V absolute maximum rating makes it easier to survive lightning surge tests (IEC61000-4-5). The soft start cap disconnect allows for the use of smaller hot swap FETs by limiting the inrush current, without hurting the transient response. The dual hot swap gate driver saves space and BOM cost in high power applications that require multiple hot swap FETs. The 400-µA sourcing current allows fast recovery, which helps to avoid system resets during lightning surge tests. The dual current limit makes it easier to pass brown outs and input steps. Finally, it offers accurate under voltage and overvoltage protection with programmable thresholds and hysteresis.

The JW7211 integrates an ORing controller, making it ideal for –48-V systems that require reverse hook-up protection and reverse-current protection. The ORing controller protects the output when the input drops avoiding system resets.

FEATURES

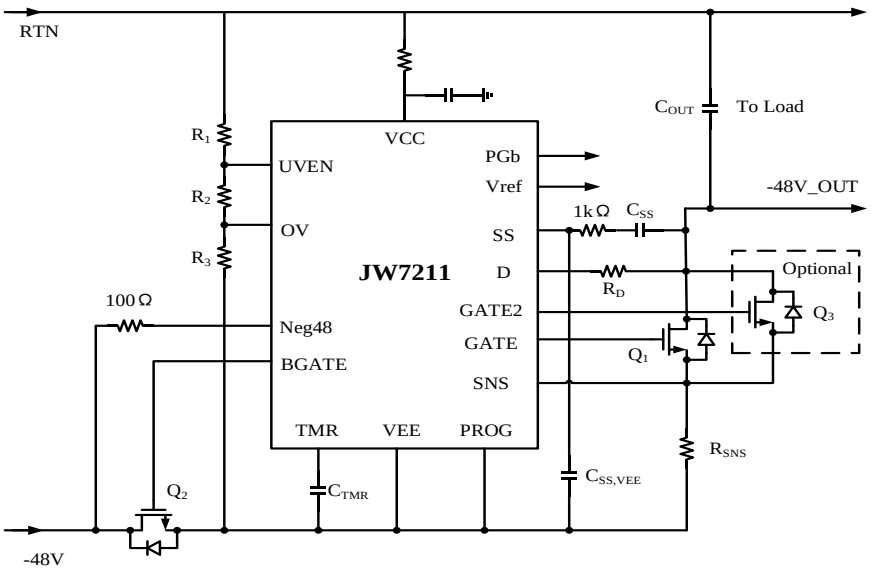
- –10V to –80V DC Operation, –200V Absolute Maximum
- Soft Start Cap Disconnect
- Dual Hot Swap Gate Drive
- 400-µA Gate Sourcing Current
- Dual Current Limit (based on VDS)
  - 24.5 mV ±10% When Low VDS
  - 3.7 mV ±27% When High VDS
- Programmable UV(±1.5%) and OV (±2%)
  - Programmable Hysteresis (±11%)
- Integrated ORing Controller
  - Regulation: 25 mV ±15 mV
  - Fast Turn off: –25 mV ±15 mV
- Retries After Time Out
- 16-Pin TSSOP

APPLICATIONS

- Remote Radio Units
- Baseband Units
- Routers and Switchers
- Small Cells
- –48-V Telecommunications Infrastructure

TYPICAL APPLICATION

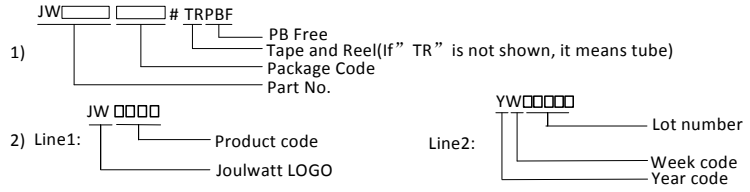
Simplified Schematic



ORDER INFORMATION

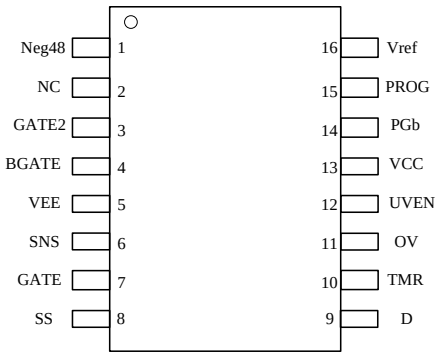
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW7211TSSOPB#TRPBF	TSSOP16	JW7211 YW□□□□□

Note：



PIN CONFIGURATION

PW Package
16-Pin (TSSOP)
TOP VIEW



Not to scale

ABSOLUTE MAXIMUM RATING[1)]

Supply Voltage----V_{VCC} (current into V_{CC} <10 mA)..... -0.3V to 20V
Input Voltage----V_{SNS}, V_{OV}.....-0.3V to 6.5V
Input Voltage---- V_{UVEN}, V_D, V_{SS}..... -0.3V to 30V
Input Voltage----V_{Neg48}..... -0.3V to 200V
Input Voltage----V_{Neg48} through 100-Ω resistor..... -1V to 200V
Input Voltage----V_{Neg48} through 1-kΩ resistor……-2V to 200V
Output Voltage----V_{GATE}, V_{GATE2},V_{BGATE} ..... -0.3V to V_{CC}
Output Voltage---- V_{TMR} , V_{PROG}, V_{VREF} ..... -0.3V to 6.5V
Output Voltage---- V_{PGb}……..... -0.3V to 200V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature, T_{stg} .....-55ºC to 150ºC

ESD Susceptibility (Human Body Model) ..... ±2kV
ESD Susceptibility (Charged Device Model) ..... ±500V

RECOMMENDED OPERATING CONDITIONS[3)]

V_{VCC}----Supply Voltage (current into V_{CC} <10 mA))..... 0V to 20V
V_{SNS}, V_{OV}.....0V to 5.5V
V_{UVEN}, V_D, V_{SS}.....0V to 18V
V_{Neg48}.....-0.2V to 150V
V_{GATE}, V_{GATE2}, V_{BGATE}..... 0V to V_{CC}
V_{TMR} , V_{PROG}, V_{VREF}.....0V to 5.5V
V_{PGb}.....0V to 80V
C_{SS}.....1nF to 200nF
R_{SS}.....1 kΩ to 10kΩ
R_D..... 120 kΩ to 2000kΩ
R_{NEG48V}..... 100 kΩ to 1kΩ
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE [4)]

$R_{\theta JA}$---Junction-To-Ambient Thermal Resistance….....98.4ºC/W
$R_{\theta JC(top)}$ ----Junction-To-Case (top) Thermal Resistance….....31.4ºC/W
$R_{\theta JB}$---Junction-To-Ambient Thermal Resistance….....44.3ºC/W
ψ_{JT} ---Junction-To-Ambient Thermal Resistance….....1.8ºC/W
ψ_{JB} ---Junction-To-Ambient Thermal Resistance….....43.6ºC/W
$R_{\theta JC(bot)}$ ---Junction-To-Ambient Thermal Resistance….....N/A

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW7211 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_J =-40°C~125°C, 1.1 mA < I_{VCC} < 10 mA, $V_{(UVEN)}$ = 2 V, $V_{(OV)}$ = $V_{(SNS)}$ = $V_{(D)}$ = 0 V, $V_{(SS)}$ = GATEx = Hi-Z , $V_{(TMR)}$ = 0 V, –1V < V_{NEG48V}x < 150 V, V_{Vref} = V_{PROG} = Hi-Z; All pin voltages are relative to V_{EE} (unless otherwise noted).

Item	Symbol	Condition	Min.	Typ.	Max.	Units
VCC – Clamped Supply						
UVLO on VCC	$V_{(UVLO\_VCC)}$	rising	9	9.5	10	V
UVLO hysteresis on VCC	$V_{(UVLO\_VCC, hyst)}$	hysteresis		1.2		V
VCC regulation	$V_{(VCC)}$	1.1< $I_{(VCC)}$ < 10 mA (current into V_{CC})	12	14.5	18	V
Quiescent Current	Quiescent Current	V_{VCC} = 10 V. Off			1	mA
		V_{VCC} = 10 V, Gate and BGATE in regulation			1.1	
UVEN – Under Voltage and Enable						
Threshold voltage for $V_{(UVEN)}$	$V_{(UVEN\_T)}$		0.985	1	1.015	V
Hysteresis current, sourcing from UV pin	$I_{(UV\_hyst)}$	V_{UV} = 1.5 V	9	10	11.2	µA
OV – Over Voltage						
Threshold voltage for V_{OV}	$V_{(OV\_T)}$		0.98	1	1.02	V
Hysteresis current, sourcing from OV pin	$I_{(OV\_hyst)}$	V_{OV} = 1.5 V	9	10	11.2	µA
TMR – Timer						
Voltage on timer when part times out.	V_{TMR}	VD = 0 V, TMR ↑, measure VTMR when VGATE = 0	1.47	1.5	1.53	V
Voltage on timer when part times out	V_{TMR2}	VD = 1 V, TMR ↑, measure VTMR when VGATE = 0	0.735	0.75	0.765	V
Timer Sourcing current when in fault condition or when retrying.	$I_{TMR,SRs}$	VSNS = 0.1 V, VD = 0 V, VTMR = 0 V, measure I out from TMR	9		12	µA
		VSNS = 0.1 V, VD = 2 V, VTMR = 0 V, measure I out from TMR	45	50	57	
Timer sinking current when not in fault condition.	$I_{TMR,SNC}$	V_{SNS} = 0 V, V_D = 0 V, V_{TMR} = 2 V,	1.5	2	2.5	µA
Voltage on timer when the timer starts going back up in retry. Retry version only.	$V_{TMR,RETRY}$	VSNS = 0 V, VD = 0 V, TMR ↑ = 2 V, TMR ↓, measure VTMR when I into TMR change polarity	0.455	0.48	0.505	V
Number of retry duty cycles. Retry version only. [5)]	N_{RETRY}			63		
Retry duty cycle. Retry version only[5)]	D_{RETRY}			0.4%		

Gate Sourcing Current Threshold When timer starts to run.	$I_{GATE,TIMER}$	V_G = 5 V, V_D = 2 V, V_{SNS} ↑, measure I_{GATE} when TMR sources current	5	10	15	uA
Sense Voltage when Timer starts to run.	$V_{SNS,TMR1}$	V_D = 2 V, V_{TMR} = 0 V, V_G = 5 V; V_{SNS} ↑, measure V_{SNS} when TMR sources current	1.5	2.5		mV
SNS – Sense Pin For Current Limit						
Leakage current on sense pin	$I_{SNS,LEAK}$		-2		2	uA
PROG = Float	$V_{SNS,CL1}$	VTMR = 0 V. VGATE = 5 V. VD = 0 V, VSNS ↑, measure when IGATE = 0;	22	24.5	27	mV
PROG = VEE			36	40	44	
PROG = Float	$V_{SNS,FST}$	VTMR = 0 V. VGATE = 5 V. VD = 0 V, VSNS ↑,measure when IGATE> 100 mA	45	50	55	mV
PROG = VEE			72	80	88	
R_{PROG} = 70kΩ			110	120	130	
R_{PROG} = 190 kΩ			68	75	82	
Fold Back Current Limit	$V_{SNS,CL2}$	V_{TMR} = 0 V, GAET =GATE2=5V, V_D = 5 V, V_{SNS} ↑, measure when I_{GATE} = 0;	2.7	3.7	4.7	mV
Fast Trip during start-up	$V_{SNS,FST2}$	V_{TMR} = 0 V, GAET =GATE2=5V, V_D = 5 V, V_{SNS} ↑, measure when I_{GATE}> 100mA	6	9	15	mV
PROG – Programing Pin to Set Current Limit (CL) and Fast Trip						
PROG pin current	i_{PROG}		9	10.25	11.5	uA
Prog pin voltage	$V_{PROG,LOW}$	Threshold on V_{PROG}, where the fast trip setting changes from 80mV to 120mV.			0.6	V
Prog pin voltage	$V_{PROG,MID}$	Threshold on V_{PROG}, where the current limit setting changes from 25mV to 40mV.	0.94	1.23	1.51	V
Prog pin voltage	$V_{PROG,High}$	Threshold on V_{PROG}, where the fast trip setting changes from 50mV to 75mV.	2.2			V
GATE – Gate Drive for Main Hot Swap FET						
Output gate voltage	$V_{(VCC-GATE)}$	$V_{(SNS)}$ = 0 V			1	V
Sourcing Current during normal operation.	$I_{(GATE,SRS,NORM)}$	$V_{(TMR)}$ = 0 V. $V_{(GATE)}$ = 8 V. V_D = 0 V, $V_{(SNS)}$ = 0 V	250	400		uA
Sourcing Current during starup	$I_{(GATE,SRS,START)}$	$V_{(TMR)}$ = 0 V. $V_{(GATE)}$ = 5 V. V_D = 0V, $V_{(SNS)}$ = 0 V	15	20	25	uA
Weak pull down current	$I_{(GATE,wkpd)}$	$V_{(SNS)}$ = 0 V. V_{UVEN} = 0 V	1.5	2.5	3.5	mA
Fast Pull down current with 10mV overdrive	$I_{(GATE,FST)}$		0.4	1	1.5	A
GATE2 – Gate Drive for Auxiliary Hot Swap FET						
Output gate voltage	$V_{(VCC-GATE2)}$	$V_{(SNS)}$ = 0 V			1	V

weak pull down	$I_{(GATE2,wkpd)}$	V_{GATE} = 0 V		4		mA
Sourcing Current	$I_{(GATE2,SRC)}$			50		uA
Fast Pull down current with 10 mV overdrive	$I_{GATE2,FST}$		0.4	1	1.5	A
Threshold on V_{GATE} when GATE2 turns on	$V_{GATE,TH}$	Raise V_{GATE}, measure when V_{GATE2} comes up.	6.25	7.25	8	V
Hysteresis of threshold on V_{GATE} when GATE2 turns on	$V_{GATE,TH,hyst}$	hysteresis		0.5		V
D – Drain Sense						
Resistance from the drain pin to GND.	$I_{(D,SNC)}$	VD=0.75V	23.7	25	27	uA
		VD=1.5V	47.5	50	55	
Voltage on drain that switches between two current limits	$V_{(D,CL\_SW)}$	$V_{(TMR)}$ = 0 V, $V_{(GATE)}$ = 5 V, $V_{(SNS)}$ =20 mV, D↑, measure V when $I_{(GATE)}$= 0	1.46	1.5	1.54	V
Voltage on drain that switches the V_{TMR} threshold.	$V_{(D,TMR\_SW)}$	$V_{(TMR)}$ = 1 V, $V_{(GATE)}$ = 5 V, $V_{(SNS)}$ =20 mV, D↑, measure V when $I_{(GATE)}$= 0	0.73	0.75	0.77	V
hysteresis for $V_{(D,TMR,SW)}$	$V_{(D,TMR\_SW,hyst)}$	hysteresis		75		mV
SS (Soft Start)						
Pull down current when not in inrush	$I_{(SS,PD)}$	GAET =GATE2=8V ,V_{SS} = 5 V	100			mA
Resistance between GATE and SS in the start-up phase	$R_{(SS,GATE)}$			80		Ω
Vref						
Reference output	V_{Vref}	0 < I_{Vref} < 1mA	4	4.9	5.5	V
V_{Vref} SC current	I_{Vref}	Vref ON, V_{Vref} (shorted)		10		mA
Neg48						
Leakage current	$I_{(lkg,Neg48)}$	V_{Neg48} = –50 mV, BGATE ON	-2		2	uA
		V_{Neg48} = –100 mV, BGATE ON	-7		7	
		V_{Neg48} = 150 V, BGATE off			30	
Forward regulation voltage of the ORing controller. V_{FWD} = V_{EE} – $V_{(NEG48Vx)}$	$V_{(FWD)}$		10	25	40	mV
Forward voltage where a fast pull up is activated.	$V_{(FWD,FST)}$	BGATE = 5 V. V_{VEE} – $V_{Neg48Vx}$ ↑ measure when I_{BGATE}= 100 μA	50	80	105	mV
Fast reverse trip voltage.	$V_{(RV)}$		10	25	40	mV
BGATE						
Gate Output Voltage	$V_{VCC-BGATE}$			0.65	1.1	V

Gate sourcing current in regulation	$I_{(BGATE,SRS)}$	$V_{VEE} - V_{Neg48Vx}$ = 50 mV		30		uA
Gate sinking current in regulation	$I_{(BGATE,SINK)}$	$V_{VEE} - V_{Neg48Vx}$ = 0		30		uA
Pull up resistance in fast sourcing mode.	$R_{GATE,SRC,FST}$	$V_{VEE} - V_{Neg48Vx}$ = 100 mV; Measure current at V_{GATEx} = 0 V. R = V_{VCC}/I		17		kΩ
Fast Gate pull down current	$I_{(BGATE,FST)}$	$V_{(VEE)} - V_{Neg48}$ = –50 mV	0.4	1	1.5	A
PGb (Power Good Bar)						
Threshold on GATE2 that triggers PGb to assert.	$V_{(GATE2,PGb)}$	Raise V_{GATE2} until PGb asserts	6.5	7.25	8	V
Pull down strength on PGb	$V_{(PGb,PD)}$	PGb sinking 1 mA			1.5	V
leakage current on PGb pin	$I_{(PGb,LEAK)}$				1	uA
OTSD (Over Temperature Shut Down)						
Shutdown temperature	T_{SD}	Temp Rising	140	160	180	ºC
Shutdown temperature Hysteresis	$T_{SD,hyst}$			18		ºC
VCC – Clamped Supply						
Insertion Delay[5)]	t_{ID}	V_{VCC}: 0 V → 10 V, measure delay before V_{GATE} ↑		32		ms
UVEN						
Deglitch on UVEN[5)]	$T_{UV,degl}$			4		us
OV						
Deglitch on OV[1)]	$T_{OV,degl}$			4		us
SNS						
Response time to large over current[5)]	$T_{SNS,FST,RESP}$	V_{SNS} steps from 0 mV to 60 mV. Measure time for GATE and GATE2 to come down.		300		ns
Neg48V						
Response time to large reverse Current[5)]	$T_{Neg48V,FST,RESP}$	V_{NEG48V} steps from -40 mV to 15 mV. Measure time for BGATE to come down.		300		ns
PGb						
Deglitch of PGb. (GATE2 =unloaded, raise GATE,measure delay between GATE and PGb) [5)]	$t_{PGb,DEGL}$	Power Good ↑ ($V_{(GATE)}$ 0 V → 10 V) Look for PGb ↓		1		ms
		Power Good ↓ ($V_{(GATE)}$ 10 V → 0 V) Look for PGb ↑		32		ms

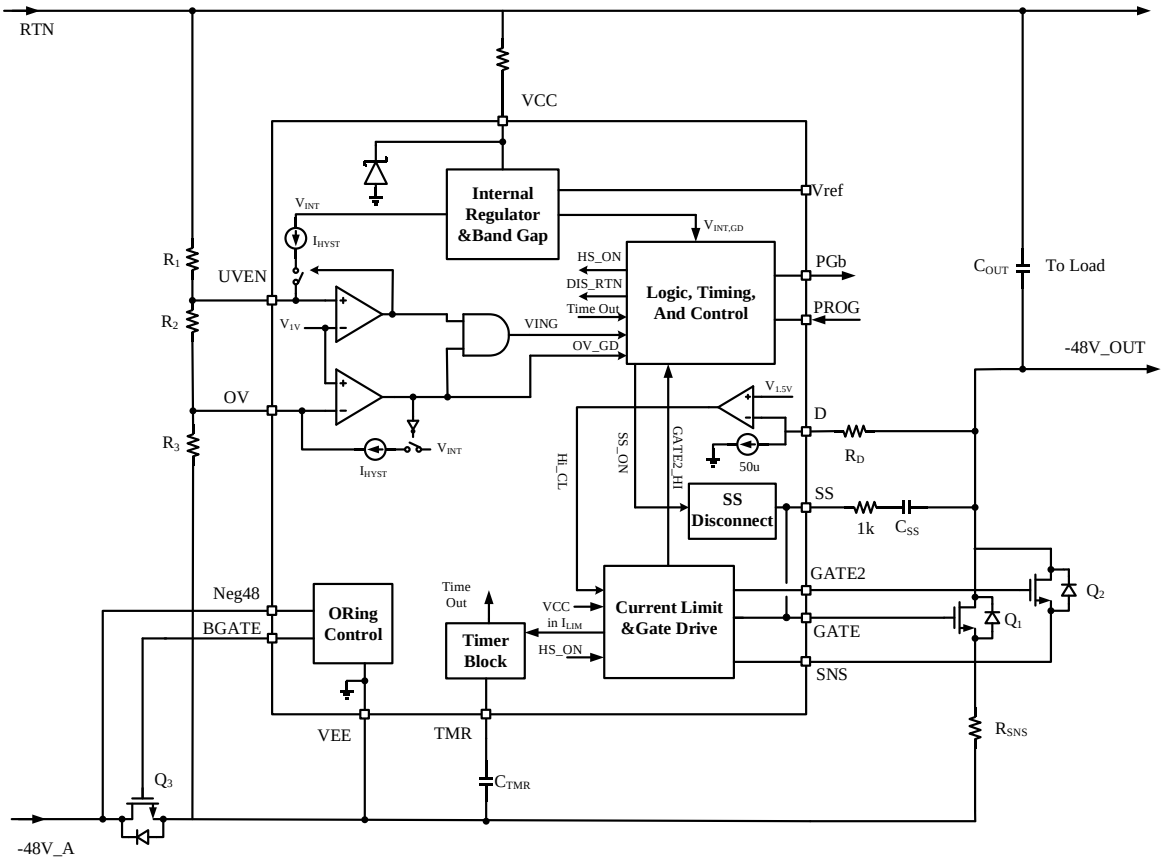
Note：

5) Guaranteed by design

PIN DESCRIPTION

Name	Pin	Description
1	Neg48	Input to the ORing controller for the –48 feed. The JW7211 will regulate the drop from VEE to Neg48 to 25 mV to mimic an ideal diode.
2	NC	No connect to space high voltage pins
3	GATE2	Gate driver for the 2nd hot swap FET. NC if feature isn't used
4	BGATE	Gate driver for the ORing FET.
5	VEE	This pin corresponds to the IC GND. Kelvin sense to the bottom of R_{SNS} to ensure accurate current limit.
6	SNS	Sense pin, used to measure current and regulate it. Kelvin Sense to R_{SNS} to ensure accurate current limits.
7	GATE	Gate drive for the main hot swap FET.
8	SS	Pin used for soft starting the output. Connect a capacitor (C_{SS}) between the SS pin and -48V_OUT. The dv/dt rate on the -48V_OUT pin is proportional to the gate sourcing current divided by C_{SS}.
9	D	Pin used to sense the drain of the hot swap FET and to program the threshold where the hot swap switches from the CL1 and CL2. Connect a resistor from this pin to the drain of the hotswap FET (also called -48V_OUT) to program the threshold.
10	TMR	Timer pin used to program the duration when the hot swap FET can be in current limit. Program this time by adding a capacitor between the TMR pin and VEE.
11	OV	Input over voltage comparator. Tie a resistor divider to program the threshold where the device turns off due to over voltage event. OV hysteresis is realized by hysteresis current and external resistor. A resistor divider over 20kΩ is recommended in typical application.
12	UVEN	Input under voltage comparator. Tie a resistor divider to program the threshold where the device turns on. UVEN hysteresis is realized by hysteresis current and external resistor. A resistor divider over 20kΩ is recommended in typical application.
13	VCC	Clamped supply. Tie to RTN through resistor.
14	PGb	Power Good Bar, which is an open drain output that indicated when the power is good and the load can start drawing full power. PGb goes low when the hot swap is fully on and the DC/DC can draw full power.
15	PROG	Adjust current limit and fast trip threshold by tying to VEE, floating, or tying to VEE through resistor.
16	Vref	5V reference output. Connect to the source of a NMOS to generate a rail that can be used to power current monitors and digital Isolators.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Overview

The JW7211 is an integrated hot swap and Single ORing controller that enables high power telecom systems to comply with stringent transient requirements. The soft start cap disconnect allows soft start at start-up and disconnects the soft start cap during normal operation. This allows for the use of smaller hot swap FETs without hurting the transient response. GATE2 is a second hot swap FET driver, which only turns ON when the main hot swap FET is fully on. Thus the FETs driven by GATE2 don't need to have strong SOA. This saves space and BOM cost in high power applications that require multiple hot swap FETs. The 400 µA sourcing current allows fast recovery, which helps to avoid system resets during lightning surge tests. Finally, the JW7211 offers accurate under voltage and over voltage protection with programmable thresholds and hysteresis.

The JW7211 integrates an ORing controller, making it ideal for –48 V systems that require reverse hook-up protection and reverse-current protection. The ORing controller protects the output when the input drops avoiding system resets. The ORing controller will turn off if any reverse current is detected.

Current Limit

The JW7211 utilizes two current limit thresholds:

- I_{CL1} – also referred to as high current limit threshold, which is used when the V_{DS} of the hot swap FET is low.
- I_{CL2} – lower current limit threshold, which is used when the V_{DS} of the hot swap FET is high.

This dual level protection scheme ensures that the part has a higher chance of riding out voltage steps and other transients due to the higher current limit at low V_{DS}, while protecting the MOSFET during start into short and hot short events, by setting a lower current limit threshold for conditions with high V_{DS}. The transition threshold is programmed with a resistor that is connected from the drain of the hot swap FET to the D pin of the JW7211. Note that compared to a traditional SOA protection scheme this approach allows better utilization of the SOA in the 10V < V_{DS} < 40V range, which is critical in riding through transients and voltage steps. Note that in both cases the JW7211 regulated the gate voltage to enforce the current limit. However, this regulation is not very fast and doesn't offer the best protection against hot-shorts on the output. To protect in this scenario a fast comparator is used, which quickly pulls down the gate in case of severe over current events (2x bigger than V_{CL1}).

Programming the CL Switch-Over Threshold

The V_{DS} threshold when the JW7211 switches over from I_{CL1} to I_{CL2} ($V_{D,SW}$) can be computed using Equation1.

$$V_{DS,SW} = 1.5V + 50\mu A \times R_D \quad (1)$$

Setting Up the PROG Pin

The PROG pin can be tied to VEE, left floating, or tied to VEE through a resistor to adjust $V_{SNS,CL1}$ and the ratio of fast trip to current limit. The options are set as follows:

- PROG = NC or Float: $V_{SNS,CL1}$ = 24.5 mV, $V_{SNS,FST}$ is 2x $V_{SNS,CL1}$
- R_{PROG} = 190 kΩ (1%): $V_{SNS,CL1}$ = 24.5 mV, $V_{SNS,FST}$ is 3x $V_{SNS,CL1}$
- R_{PROG} = 70 kΩ (1%): $V_{SNS,CL1}$ = 40 mV, $V_{SNS,FST}$ is 3x $V_{SNS,CL1}$
- PROG = VEE: $V_{SNS,CL1}$ = 40 mV, $V_{SNS,FST}$ is 2x $V_{SNS,CL1}$

Programming CL1

The current limit at low V_{DS} (I_{CL1}) of the JW7211 can be computed using Equation 2 below.

$$I_{CL1} = \frac{V_{SNS,CL1}}{R_{SNS}} \quad (2)$$

Programming CL2

The current limit at high V_{DS} (I_{CL2}) of the JW7211 can be computed using Equation 3 below.

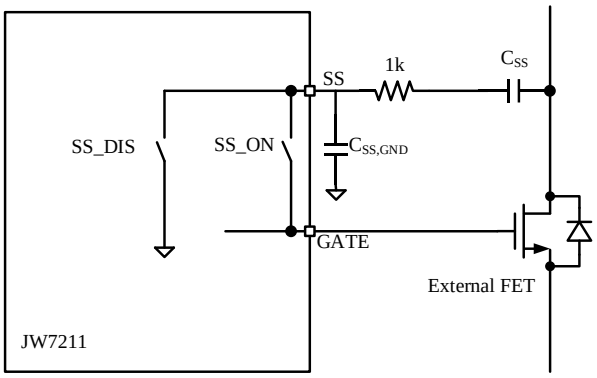
$$I_{CL2} = \frac{V_{SNS,CL2}}{R_{SNS}} \quad (3)$$

Soft Start Disconnect

The inrush current into the output capacitor (C_{OUT}) can be limited by placing a capacitor between the SS (Soft Start) pin and the drain of the hot swap MOSFET. In that case the inrush current can be computed using equation below.

$$I_{INR} = \frac{C_{OUT} \times I_{GATE,SRS,START}}{C_{SS}} \quad (4)$$

Note that with most hot swap the C_{SS} pin is tied simply to the gate pin, but this can interfere with performance during normal operation if transients or short circuits are encountered. In addition the C_{SS} capacitor tends to pull up the gate during hot plug and cause shoot through current if it is always tied to the gate. For that reason the JW7211 has a disconnect switch between the gate pin and the SS pin as well as a discharge resistor. During the initial hot plug and during the insertion delay the switch between SS and GATE is open and SS is being discharged to GND through a resistor. Then during start-up SS and GATE are connected to limit the slew rate. Once in normal operation the SS pin is not tied to GATE and it is not shorted to GND, which prevents it from interfering with the operation during transients.



Implementation of SS Disconnect

Timer

Timer is a critical feature in the hot swap, which manages the stress level in the MOSFET. The timer will source
and sink current into the timer capacitor as follows:

- Not in current limit: sink 2 μA
- If the part is in current limit and V_{GATE} < $V_{GATE,TH}$, the timer sources current as follows:
  – V_D < V_{D,CL_SW}: source 10 μA
  – V_D > V_{D,CL_SW}: source 50 μA

The JW7211 times out and shuts down the hot swap as follows.

- If V_D < V_{D,TMR_SW} then the hot swap times out when V_{TMR} reaches 1.5 V.
- If V_D > V_{D,TMR_SW} then the hot swap times out when V_{TMR} reaches 0.75 V.

The above behavior maximizes the ability of the hot swap to ride out voltage steps, while ensuring that the FET remains safe even if the part can not ride out a voltage step.

- A cool down period follows after the part times out. During this time the timer performs the following:
- Discharge C_{TMR} with a 2-μA current source until 0.5 V
- Charge C_{TMR} with a 10-μA current source until it is back to 1.5 V.
- Repeat the above 63 times
- Discharge timer to 0 V.

The part attempts to restart after finishing the above. If the UVEN signal is toggled while the 63 cycles are in progress the part restarts

immediately after the 63 cycles are completed. The timer operates as follows when recovering from POR:

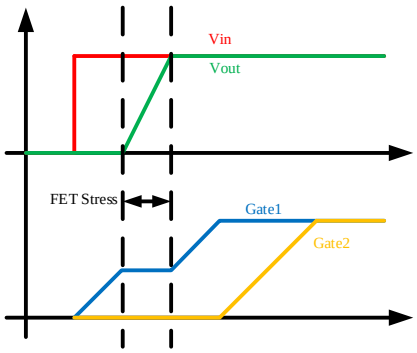
- If V_{TMR} < 0.5 V:
  – Proceed to regular startup
  – Do not discharge V_{TMR}
- If V_{TMR} > 0.5 V:
  – Go through 63 charge/discharge cycles
  – Discharge V_{TMR}
  – Proceed to startup

The Time Out (T_{TO}) can be computed using the equations below. Note that the time out depends on the V_{DS} of the MOSFET.

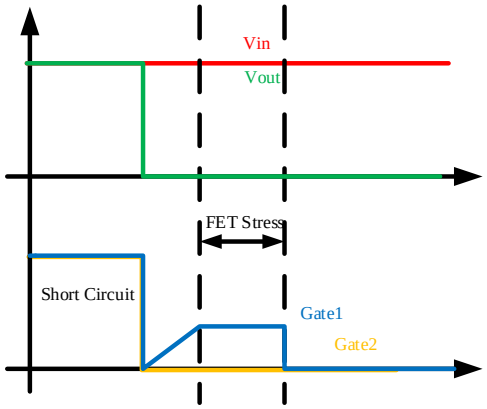
$$T_{TO} = \frac{C_{TMR} \times V_{TMR}}{I_{TMR,SRS}} \quad (5)$$

Gate 2

The JW7211 features a second hot swap Gate drive, which can be used to save BOM cost and size in applications that require multiple hot swap MOSFETs. The 2nd MOSFET is only turned ON when the main FET is enhanced. As a result the 2nd MOSFET doesn't operate with large current and large voltage across it, thus reducing the SOA requirements. The following figures show the operation during start-up and Hot Short event. It can be seen that the second FET is OFF during stressful operation and turns on during normal operation to improve steady state efficiency and reduce power losses.



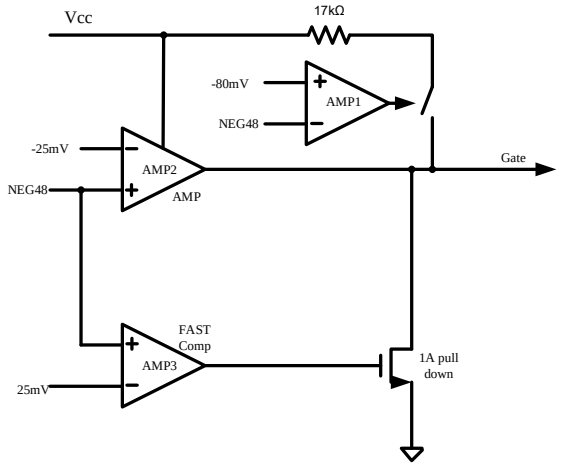
Gate2 Operation During start-up



Gate2 Operation During Hot Short

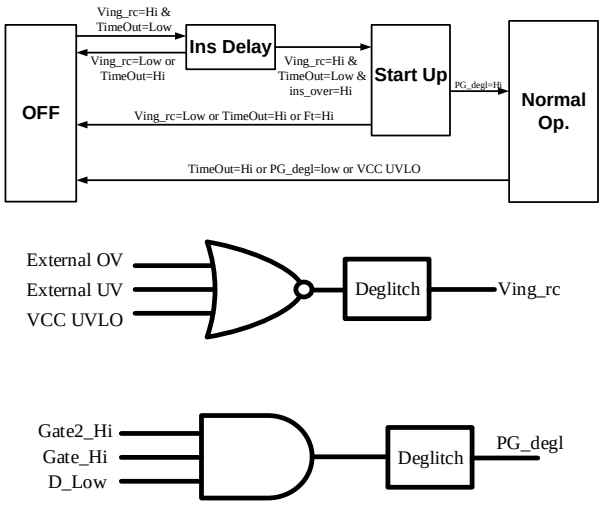
ORing

The JW7211 features integrated ORing that controls the external MOSFET in a way to emulate an ideal diode. The JW7211 will regulate the forward drop across the ORing FET to 25 mV. This is accomplished by controlling the V_{GS} of the MOSFET. As the current decreases the V_{GS} is also decreased, which effectively increases the R_{DSON} of the MOSFET. This process is regulated with a low gain amplifier that is gate (ORing FET) pole compensated. The lower gain helps ensure stability over various operating conditions. The regulating amplifier ensures that there is no DC reverse current. However, the amplifier is not very fast and thus it is paired with a fast comparator. This comparator quickly turns off the FET if there is significant reverse current detected.



Simplified Diagram of or-ing block

Device Functional Modes



Simplified Hot Swap State Machine

The Figure above shows a simplified state machine of the hot swap controller. It has 4 distinct operating states and the controller switches between these states based on the following signals:

- Ving_rc: This means that both the input voltage is in the right range and the IC has power with Vcc. If the input voltage is above the OV threshold, input voltage is below the UV threshold, or VCC is below its internal UVLO, Ving_rc will be low.
- TimeOut: This signal comes from the timer block and will be asserted Hi if the IC has timed out due to an over-current condition. This signal is also Hi while the timer is going through the restart cycles. Once the cycles are completed this signal will go Low.
- ins_over: This signal states that the insertion delay has been completed and the hot swap is ready to start-up.
- FT: this is the fast trip signal coming from the fast trip comparator. It goes Hi if an extreme over current event is detected.
- PG: Internal Power good signal. This is high when the hot swap is fully on and the load can draw full power. For PG to be Hi, the GATE has to be Hi, GATE2 needs to be Hi, and the drain pin needs to be below 0.75 V.
- PG_degl: This is a deglitched version of the PG and is the signal used to move between states and controls the external PGb pin.

OFF State

In this state the hot swap FET is turned off and the controller is waiting to start-up. The controller can be in this state due to any of these scenarios:

- Input voltage is not in the valid range.
- The hot swap is in the cool down state and the timer is going through the retry cycle after a fault condition such as output hot short or over current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Insertion Delay State

In this state the hot swap FET is turned off and the controller is waiting for the insertion delay to finish. This allows the input supply to settle after a Hot Plug. If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Once the insertion delay is finished, the controller will move to the Start-up state.

Start-up State

In this state the controller is turning on and charging the output cap. The operation is set as follows:

- The SS pin is internally connected to the GATE pin to allow for output dv/dt control.
- Lower gate sourcing current is applied to the GATE pin to allow for smaller SS caps.
- The lower current limit setting of $V_{SNS,CL2}$ and a lower fast trip setting of $V_{SNS,FST2}$ is used to minimize the MOSFET stress in case of a fault condition.

If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.
- Fast trip is triggered.

Once the PG_degl signal goes Hi, the controller will move to the Normal Operation state.

Normal Operation State

- The SS pin is disconnected from the GATE pin to improve transient response.
- The full gate sourcing current is used to improve transient response.
- The current limit and fast trip threshold are a function of the D pin to optimize the transient response while protecting the MOSFET.

If any of the following occur, the controller will be kicked back to the OFF state:

- PG_degl goes low.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Note that if the input voltage is outside the valid range or the fast trip is triggered, the hot swap FET will turn off, but the controller will not exit the Normal Operation state. In this case the PG signal would go low immediately. If this condition persists, the PG_degl will go low as well and the controller would move to the OFF state. This operation prevents the controller from re-starting the system during quick transients.

APPLICATION IMFORMATION

RSNS Selection

Before selecting RSNS. First compute the maximum load current Imax. To provide some margin, set the target current limit ICL1 to 1.2×Imax and compute RSNS using equation below:

$$R_{SNS} = \frac{V_{SNS,CL1}}{1.2 \times I_{\max}}$$

CSS and CSS, VEE Selection

First, compute the minimum inrush current where the timer will trip using equation below

$$I_{INR,TMR} = \frac{V_{SNS,\mathrm{TMR}\,2}}{R_{SNS}} = \frac{1.5mV}{R_{SNS}}$$

To avoid running the timer the inrush current needs to be sufficiently low. $I_{INR,TGT}$ below 0.8 $I_{INR,TMR}$ is recommended. In typical application Target half of $I_{INR,\ TMR}$ to allow margin, and compute the target CSS using equation below

$$C_{SS} = \frac{C_{out} \times I_{GATE,SRS,START}}{I_{INR,TGT}} = \frac{C_{out} \times 20uA \times R_{SNS}}{1.5mV / 2}$$

For example. Cout=680uF R_{SNS}=5mΩ，C_{SS} can be calculated as 90.66nF. Than choose available CSS greater than 90.66nF. For example 100nF was used. This results in an inrush current of 0.136A. Also it is recommended to add a capacitor between the soft start pin capacitor that is 3×larger than C_{SS}. In this case a 300nF capacitor was chosen.

Finally the start-up time at maximum input voltage can be computed using the equation below. For example Vin=48V. C_{SS}=100nF. TSTART can be calculated as

$$T_{START} = \frac{C_{SS} \times V_{in}}{I_{GATE,SRS,START}} = \frac{100nF \times 48V}{20uA} = 240ms$$

RD and VDS Switch Over threshold Selection

The VDS threshold where the current limit switched from CL1 to CL2 can be programmed using external resistor R_D. In general a higher threshold improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because the larger current limit is now allowed at higher VDS voltages. If there are no specific voltage step requirements, 20 V is a good starting point. Use the equation below to compute the target R_D.

$$R_D = \frac{V_{DS.SW} - 1.5V}{50uA} = \frac{20V - 1.5V}{50uA} = 370k\Omega$$

Timer Selection

The timer determines how long the hot swap can be in current limit before timing out and can be programmed using C_{TMR}. In general a longer time out (T_{TO}) improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because it takes longer for the FET to shut down during fault conditions. If there are no specific voltage step or transient requirements, 2 ms is a good starting point. Use the equation below to compute the target C_{TMR}. Choose the next available

$$C_{TMR} = \frac{T_{TO} \times I_{TMR,SRS}}{V_{TMR}}$$

MOSFET Selection and SOA Checks

When selecting MOSFETs the three key parameters are: VDS rating, RDSON, and safe operating area (SOA). For example the CSD19535KTT was selected for-48V system to provide a 100 V VDS rating, low RDSON, and sufficient SOA. After selecting the MOSFET, it is

important to double check that it has sufficient SOA to handle the key stress scenarios: start-up, output Hot Short, and Start into Short. MOSFET's SOA is usually specified at a case temperature of 25 ℃ and should be derated based on the maximum case temperature expected in the application. Compute the maximum case temperature using the equation below. Note that the RDSON will vary with temperature and solving the equation below could be a repetitive process. The CSD19535KTT, has a maximum 3.4 mΩ RDSON at room temperature and is ~1.5x higher at 100°C. N stands for the number of MOSFETs used in parallel.

$$T_{C.MAX} = T_{A.MAX} + R_{\theta CA} \times {I_{LOAD.MAX}}^2 \times R_{DSON}(\mathrm{T}_J)$$

$$T_{C.MAX} = 85℃ + 20℃/\mathrm{W} \times 5^2 \times (3.4 \times 1.5\,\mathrm{m\Omega}) = 87.5℃$$

Next the stress the MOSFET will experience during operation should be compared to the FETs capability. First, consider the power up. The inrush current with max COUT will be 0.136 A and the inrush will last for 240 ms. Note that the power dissipation of the FET will start at VIN,MAX × IINR and reduce to zero as the VDS of the MOSFET is reduced. The SOA curve of a typical MOSFET assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where PFET = VIN,MAX × IINR for t = Tstart-up /2. In this instance, the SOA can be checked by looking at a 48 V, 1.5 A, 12 ms pulse. Based on the SOA of the CSD19535KTT, it can handle 48 V, 1.8 A for 10 ms and it can handle 48V, 1 A for 100 ms. The SOA at TC = 25°C for 240ms can be extrapolated by approximating SOA vs time as a power function as shown in equations below:

$$I_{SOA}(\mathrm{t}) = a \times t^m$$

$$m = \frac{\ln(\mathrm{I}_{SOA}(\mathrm{t}_1) / \mathrm{I}_{SOA}(\mathrm{t}_2))}{\ln(\mathrm{t}_1 / \mathrm{t}_2)} = \frac{\ln(1.8\,\mathrm{A}/1\,\mathrm{A})}{\ln(10/100)} = -0.25$$

$$a = \frac{\mathrm{I}_{SOA}(\mathrm{t}_2)}{{t_2}^m} = \frac{1A}{(100ms)} = 3.16A \times ms^{0.25}$$

$$I_{SOA}(240\,\mathrm{ms}, 25℃) = a \times t^m = 0.8A$$

Finally, the FET SOA needs to be derated based on the maximum case temperature as shown below.

$$I_{SOA}(240\,\mathrm{ms}, T_{C,MAX}) = 0.8A \times \frac{175℃\text{-}87.5℃}{175℃\text{-}25℃} = 0.47A$$

Input capacitor, input TVS, and ORing FET Selection

For example, an application needs to pass a 2 kV, 2Ω lightning strike per IEC61000-4-5. This equates to almost 1000 A of input current that needs to be clamped. In addition, the design needs to pass reverse hook up and thus the TVS needs to be bi directional. A ceramic transient voltage suppressor (2x B72540T6500S162) T2220K50E2G was used to clamp this huge surge of current. According to it's datasheet it can clamp 500 A of current to 150 V. Note that the lightning strike can be positive or negative. ove RTN). If the output of the OR-ing is –48 V and the input goes to +150 V that is a 200 V drop. Thus BSC320N20NS3 was chosen for the ORing FETs. This is a 200 V FET with a 32 mΩ RDSON at room temperature. 2 of these were used in parallel to minimize power loss and manage thermal. Finally a 0.1 µF input bypass cap is recommended.

Under Voltage and Over Voltage Settings

Both the threshold and hysteresis can be programmed for under voltage and over voltage protection. In general the rising UV threshold should be set sufficiently below the minimum input voltage and the falling OV threshold should be set sufficiently above the maximum input voltage to account for tolerances. For example a rising UV

threshold of 30 V and a falling UV threshold of 28 V was chosen as the target. First, choose RUV1 based on the 2 V UV hysteresis as shown below.

$$R_{UVH} = \frac{V_{UV,hyst,tgt}}{i_{UV,hyst}} = \frac{2V}{10uA} = 200k\Omega$$

Once RUVH is known RUVL can be calculated based on the target rising UV threshold as shown below

$$R_{UVL} = \frac{R_{UVH}}{V_{UV,rise,tgt} - 1V} = \frac{200k\Omega}{30V - 1V} = 6.9k\Omega$$

For example, a rising OV threshold of 76 V and a falling UV threshold of 74 V was chosen as the target. The OV setting can be programed in a similar way as shown in equations below

$$R_{OVH} = \frac{V_{OV,hyst,tgt}}{i_{OV,hyst}} = \frac{2V}{10uA} = 200k\Omega$$

$$R_{OVL} = \frac{R_{OVH}}{V_{OV,rise,tgt} - 1V} = \frac{200k\Omega}{76V - 1V} = 2.67k\Omega$$

Optional filtering capacitors can be added to the UV and OV to improve immunity to noise and transients on the input bus. In general, a resistor divider above 20kΩ is recommended in typical application.

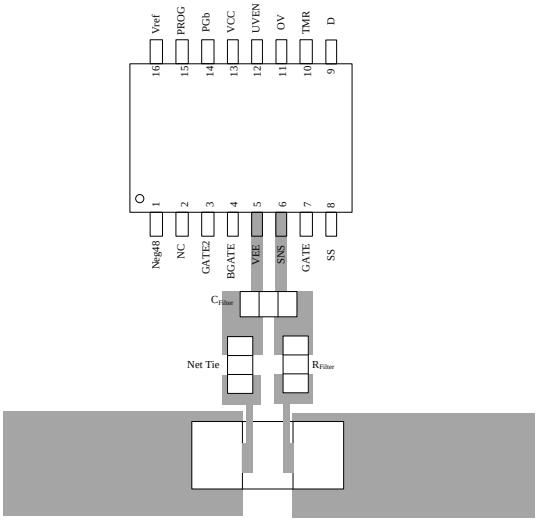
RVCC and CVCC Selection

The VCC is used as internal supply rail and is a shunt regulator. To ensure stability of internal loop a minimum of 0.1 µF is required for CVCC. To ensure reasonable power on time it is recommended to keep CVCC below 1 µF. RVCC should be sized in such a way to ensure that sufficient current is supplied to the IC at minimum operating voltage corresponding to the falling UV threshold. To allow for some margin it is recommended that the current through RVCC is at least 1.2x of IQ,MAX when RTN = Falling UV threshold and VCC = 10 V (minimum recommended operating voltage on VCC).

PCB Layout Note

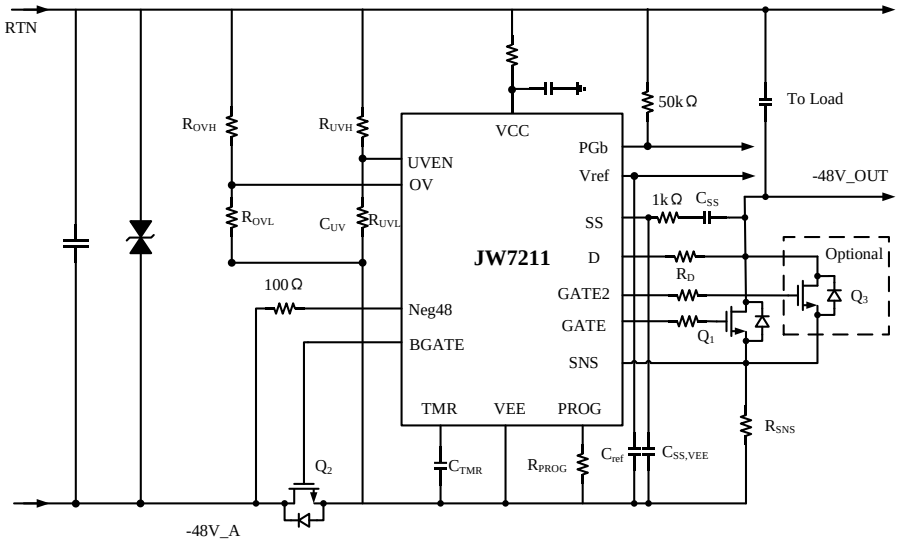
For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

- The VEE and SNS pin need to hace a Kelvin Sense connection to the sense resistor
- The VEE trace carries current and needs to be thick and short in order to minimize IR drop and to avoid introducing current sensing error
- It is recommended to use a net-tie to separate the power plane coming into the RSNS and the Kelvin connection to VEE
- Connect the Neg48Vx filtering caps, UVEN resistor divider, OV resistor divider, and TMR cap to the VEE to insure maximum accuracy.
- The filtering caps on Neg48V and SNS should be placed as close to the IC as possible

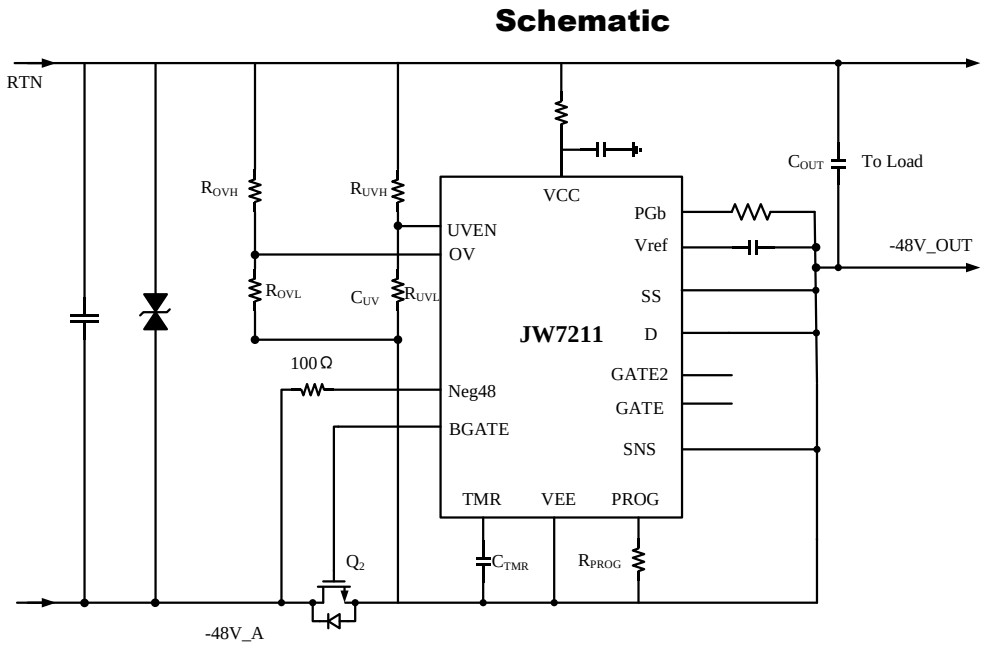


REFERENCE DESIGN

Reference1: Both or-ing and hot-swap function are used

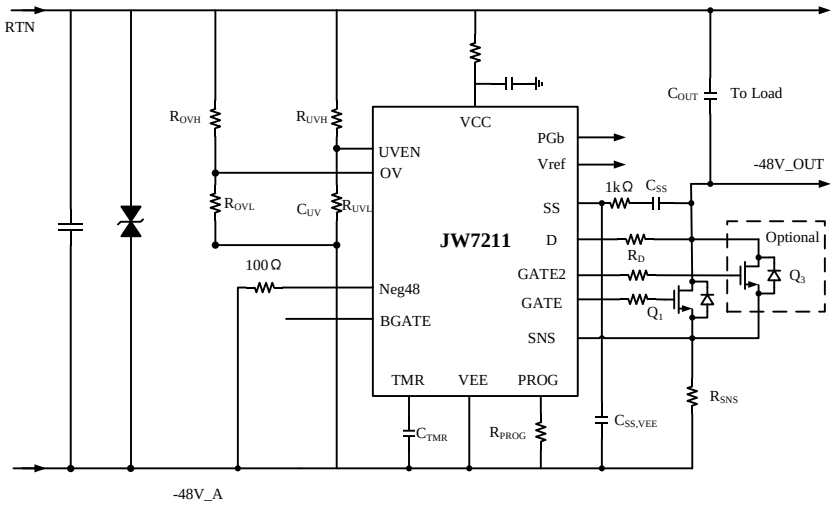


Reference2: Only or-ing control function is used



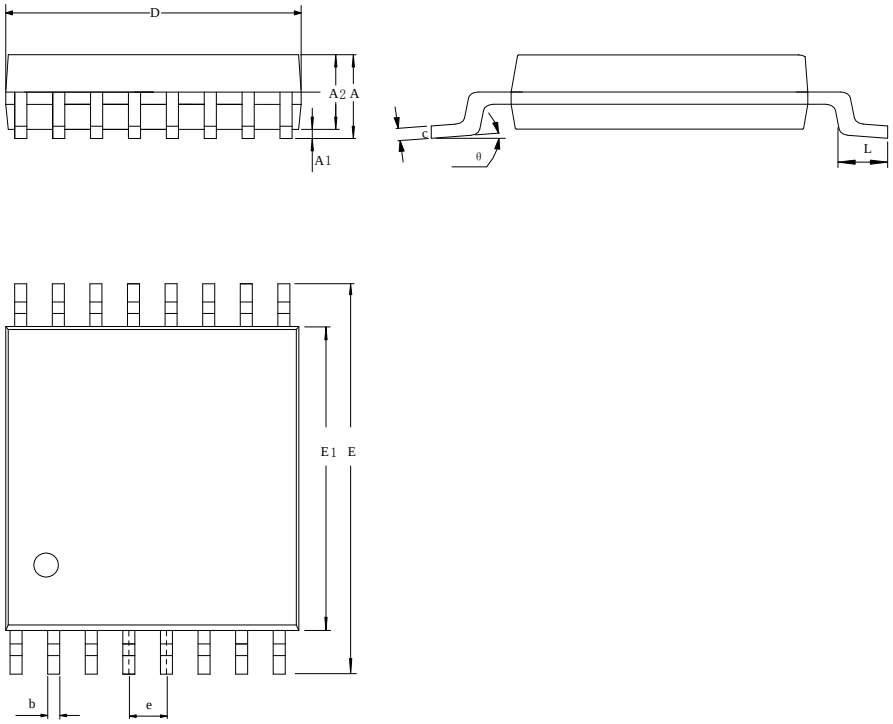
Reference2: Only hot-swap control function is used

Schematic



PACKAGE OUTLINE

TSSOP16 UNIT: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.00
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	0.65(BSC)		
L	0.50	—	0.70
θ	0°	—	8°

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